

Compal Confidential

**EH50F/EH51F
EH5VF/EH70F**

MB Schematic Document

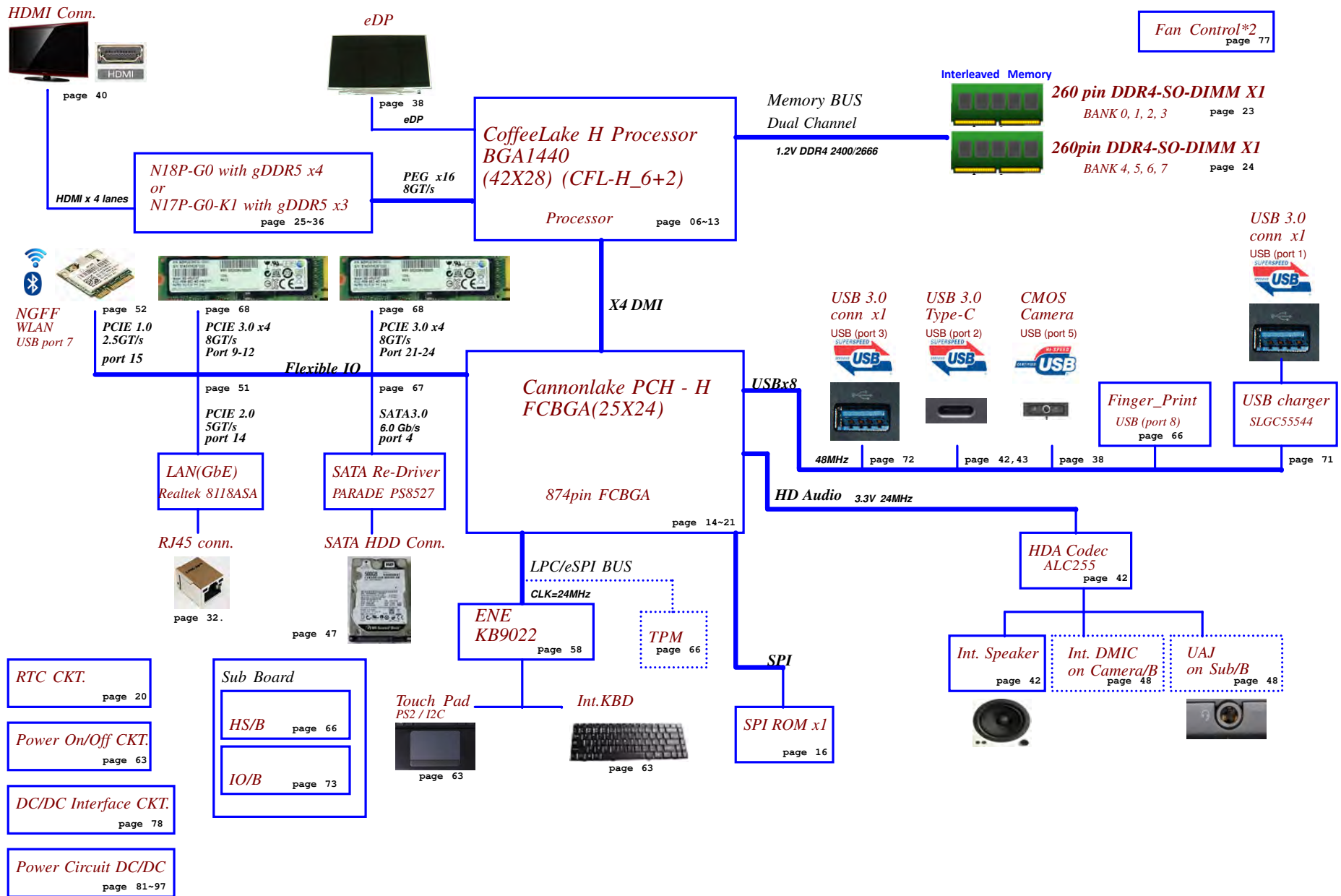
LA-H501P

Rev:1A

2019.02.22

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				Date: Friday, February 22, 2019	Rev 1A
				Sheet 1 of 101	



Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2017/07/20	Deciphered Date	2018/07/20	Block Diagrams	
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				Document Number	1A
				EHSVF M/B LA-H501P	
				Date: Friday, February 22, 2019	Sheet 2 of 101

Vcc	3.3V +/- 5%				
Ra	100K +/- 1%				
Board ID	Rb	V _{BI} D min	V _{BI} D typ	V _{BI} D max	EC AD
0	0		0.000 V	0.300 V	0x00 - 0x13
1	12K +/- 1%	0.347 V	0.345 V	0.360 V	0x14 - 0x1E
2	15K +/- 1%	0.423 V	0.430 V	0.438 V	0x1F - 0x25
3	20K +/- 1%	0.541 V	0.550 V	0.559 V	0x26 - 0x30
4	27K +/- 1%	0.691 V	0.702 V	0.713 V	0x31 - 0x3A
5	33K +/- 1%	0.807 V	0.819 V	0.831 V	0x3B - 0x45
6	43K +/- 1%	0.978 V	0.992 V	1.006 V	0x46 - 0x54
7	56K +/- 1%	1.169 V	1.185 V	1.200 V	0x55 - 0x64
8	75K +/- 1%	1.398 V	1.414 V	1.430 V	0x65 - 0x76
9	100K +/- 1%	1.634 V	1.650 V	1.667 V	0x77 - 0x87
10	130K +/- 1%	1.849 V	1.865 V	1.881 V	0x88 - 0x96
11	160K +/- 1%	2.015 V	2.031 V	2.046 V	0x97 - 0xA4
12	200K +/- 1%	2.185 V	2.200 V	2.215 V	0xA5 - 0xAF
13	240K +/- 1%	2.316 V	2.329 V	2.343 V	0xB0 - 0xB7
14	270K +/- 1%	2.395 V	2.408 V	2.421 V	0xB8 - 0xBF
15	330K +/- 1%	2.521 V	2.533 V	2.544 V	0xC0 - 0xC9
16	430K +/- 1%	2.667 V	2.677 V	2.687 V	0xCA - 0xD4
17	560K +/- 1%	2.791 V	2.800 V	2.808 V	0xD5 - 0xDD
18	750K +/- 1%	2.905 V	2.912 V	2.919 V	0xDE - 0xF0
19	NC	3.000 V	3.000 V		0xF1 - 0xFF

BUS	Device	Address(7 bit)	Address(8bit)	
			Write	Read
I2C_0 (+3VS)				
I2C_1 (+3VS)	TM-P3393-003 (Touch Pad)			
	SA577C-12A0 (Touch Pad)			
PCH_SMBCLK (+3VS)	DIMM1			
	DIMM2			
PCH_SML1CLK EC_SMB_CK2 (+3VS)	N18P-G0/N17P-G0-K1 (VGA)	0x9E		
	Thermal Sensor (W83L771)	1001_100xb	1001_1001b	1001_1000b
	PCH	0x90		
EC_SMB_CK1 (+3VLP)	BQ24780 (Charger IC)	0x12		
	BATTERY PACK	0x16		
EC_SMB_CK3 (+3VALW)	LED driver	0xC0		

[illegible]

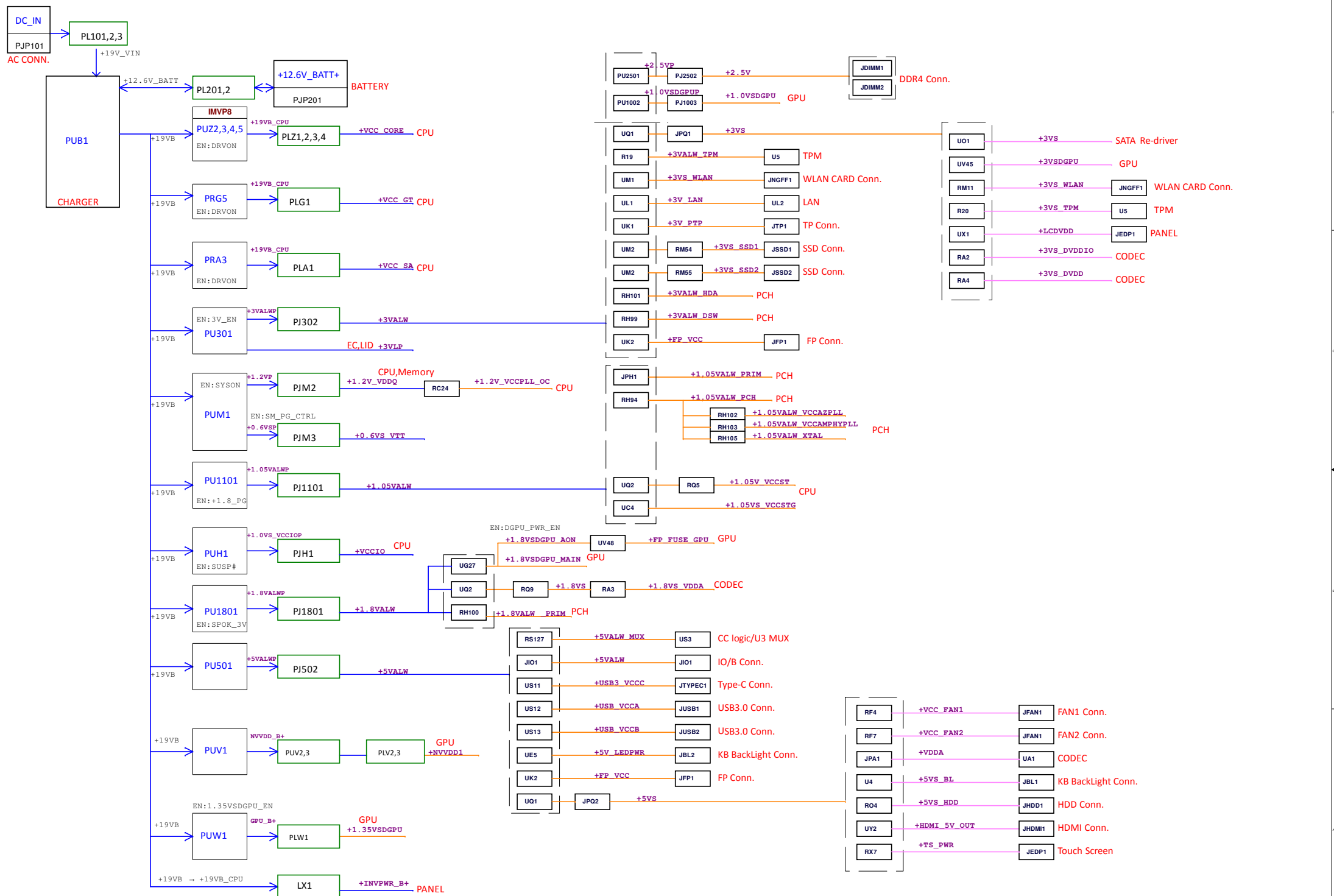
BOM Option Table	
Item	BOM Structure
Unpop	@
Connector	CONN@
CMC	CMC@
dGPU circuit	VGA@
N18P GPU	N18P@
N17P GPU	N17P@
TPM	TPM@
For Acer IOAC	IOAC@
No Acer IOAC	NIOAC@
KB backlight	KBLED@
KB LED driver	LED14P@
OVRM-ON	ON_X76@
OVRM-uPI	uPI_X76@
Thermal sensor	TMS@
for SW debug board	UART@
Intel CNVi	CNVi@
Finger Print	FP@
FinerPrint(with PBA)	PBA@
EMI requirement	EMI@
EMI require reserve	XEMI@
ESD requirement	ESD@
ESD require reserve	XESD@
FP ESD requirement	FPESD@
Pidgey ESD requirement	PGESD@
SATA HDD W REDRIVER	SATARD@
SATA HDD WO REDRIVER	SATANRD@
i5 CPU	i5@
i7 CPU	i7@
H62 CPU	H62@
H82 CPU	H82@
LAN LDO mode	LDO@
LAN Switch mode	SWR@

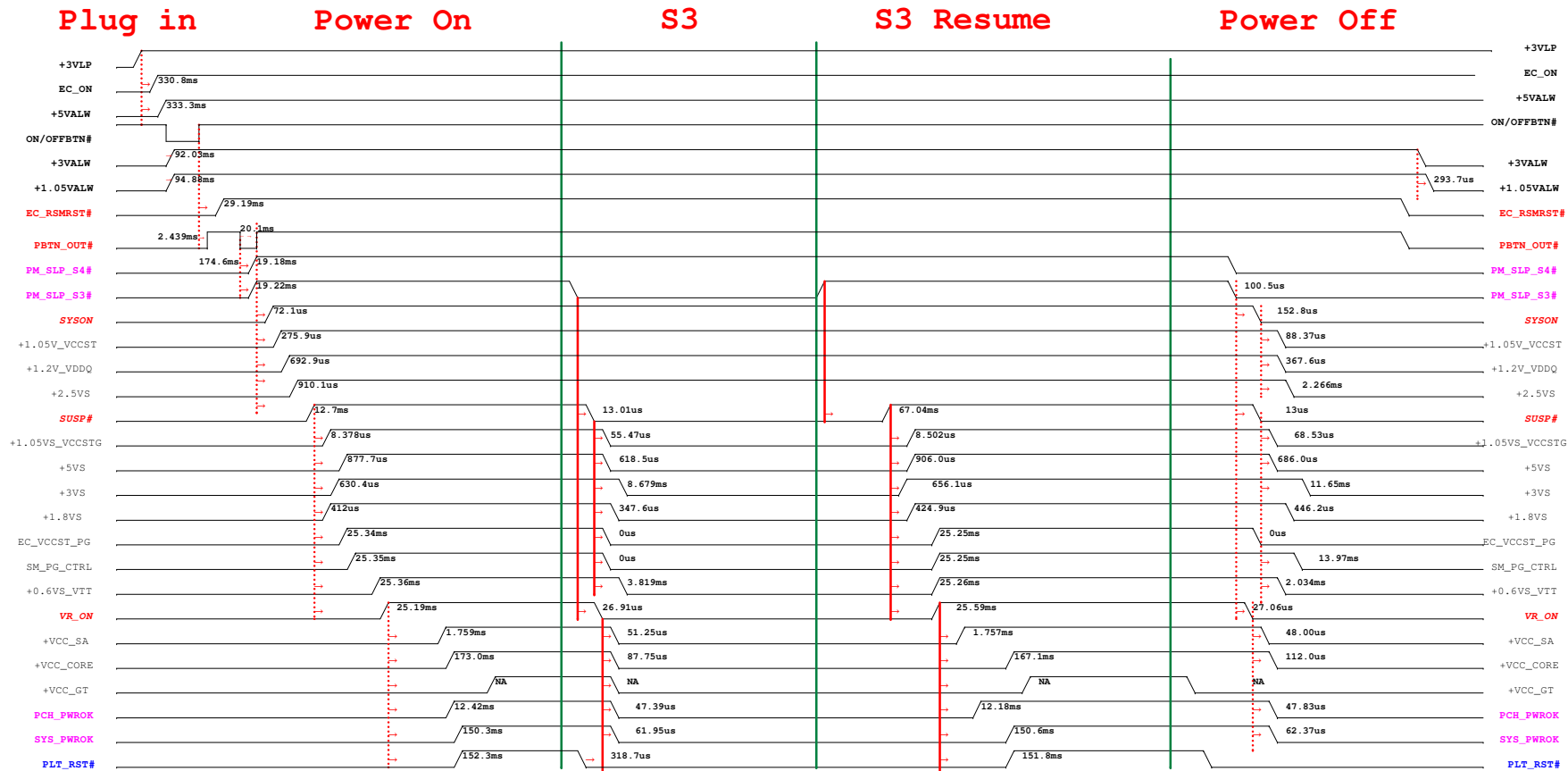
<i>SIGNAL</i>	<i>SLP_S3#</i>	<i>SLP_S4#</i>	<i>SLP_S5#</i>	<i>+VALW</i>	<i>+V</i>	<i>+VS</i>	<i>Clock</i>
<i>S0 (Full ON)</i>	<i>HIGH</i>	<i>HIGH</i>	<i>HIGH</i>	<i>ON</i>	<i>ON</i>	<i>ON</i>	<i>ON</i>
<i>S3 (Suspend to RAM)</i>	<i>LOW</i>	<i>HIGH</i>	<i>HIGH</i>	<i>ON</i>	<i>ON</i>	<i>OFF</i>	<i>OFF</i>
<i>S4 (Suspend to Disk)</i>	<i>LOW</i>	<i>LOW</i>	<i>HIGH</i>	<i>ON</i>	<i>OFF</i>	<i>OFF</i>	<i>OFF</i>
<i>S5 (Soft OFF)</i>	<i>LOW</i>	<i>LOW</i>	<i>LOW</i>	<i>ON</i>	<i>OFF</i>	<i>OFF</i>	<i>OFF</i>

Power Plane	Description	S0	S3	S4	S5
+RTCVCC	RTC Battery Power	ON	ON	ON	ON
+19V_VIN	Adapter power supply	N/A	N/A	N/A	N/A
+12.6V_BATT	Battery power supply	N/A	N/A	N/A	N/A
+19VB	AC or battery power rail for power circuit.	N/A	N/A	N/A	N/A
+3VLP	+19VB to +3VLP power rail for suspend power	ON	ON	ON	ON
+5VALW	+5V Always power rail	ON	ON	ON	ON
+3VALW	System +3VALW always on power rail	ON	ON	ON	ON*
+3VALW_DSW	+3VALW power for PCH DSW rails	ON	ON	ON	ON
+1.05VALW	+1.05V Always power rail	ON	ON	ON	ON
+1.2V_VDDQ	DDR4 +1.2V power rail	ON	ON	OFF	OFF
+1.05V_VCCST	Sustain voltage for processor in Standby modes	ON	ON	OFF	OFF
+5VS	System +5V power rail	ON	OFF	OFF	OFF
+3VS	System +3V power rail	ON	OFF	OFF	OFF
+1.05VS_VCCSTG	+1.05VALW_PRIM Gated version of VCCST	ON	OFF	OFF	OFF
+0.6VS_VTT	DDR +0.6VS power rail for DDR terminator .	ON	OFF	OFF	OFF
+VCC_CORE	Core voltage for CPU	ON	OFF	OFF	OFF
+VCC_GT	Sliced graphics power rail	ON	OFF	OFF	OFF
+VCCIO	CPU IO +0.95VS power rail	ON	OFF	OFF	OFF
+VCC_SA	System Agent power rail	ON	OFF	OFF	OFF
+1.8VSDGPU_AON	+1.8VS power rail for GPU(AON rails)	ON	OFF	OFF	OFF
+1.8VSDGPU_MAIN	+1.8VS power rail for GPU GC6	ON	OFF	OFF	OFF
+NVVDD1	Core voltage for VGA (merge core & core_s)	ON	OFF	OFF	OFF
+1.35VSDGPU	+1.35VS power rail for GPU	ON	OFF	OFF	OFF
+1.0VSDGPU	+1.0VS power rail for GPU	ON	OFF	OFF	OFF
+1.8VALW	System +1.8VALW always on power rail	ON	ON	ON	ON*

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.

Board ID	PCB Revision	Board ID	PCB Revision
0	2050 Rev0.1	10	
1	2050 Rev0.2	11	
2	2050 Rev0.3	12	
3	2050 Rev1.0/1A	13	
4	2060 Rev0.1	14	
5	2060 Rev0.2	15	
6	2060 Rev0.3	16	
7	2060 Rev1.0	17	
8		18	
9		19	



BIOS ver: V0.02W1
EC: ver: V002AT04



PCB EH5VF LA-H501P LS-H501P/H502P
DAZ2K700100



PCB EH5VF LA-H501P LS-H501P/H502P
DAZ2K700101

Coffee Lake-H CPU SKU



S IC CL8068403373522 SR3Z0 U0 2.3G ABO!
SA0000BPJ40



S IC CL8068404121905 QRR5 U0 2.4G FCBGA
SA0000COG00



S IC CL8068403359524 SR3YY U0 2.2G ABO!
SA0000BPZ40



S IC CL8068404121817 QRR2 U0 2.6G FCBGA 1440
SA0000COF10



S IC CL8068403373522 QP89 U0 2.3G BGA
SA0000BPJ10

Cannon Lake PCH SKU



S IC FH82HM370 SR40B B0 BGA 874P PCH-H ABO!
SA0000BVP10



S IC FH82HM370 QNYF B0 BGA 874P PCH-H
SA0000BPF10

NV GPU SKU



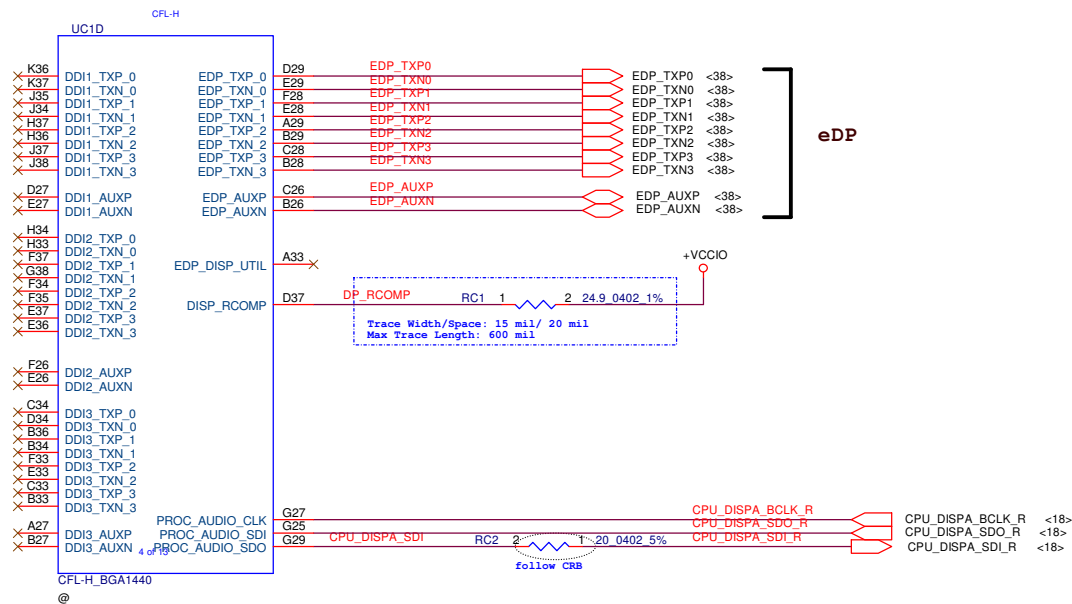
S IC N17P-G0-K1-A1 FCBGA 908P GPU ABO !
SA0000CFM20



S IC N18P-G0-A1 QS FCBGA 960P GPU ABO !
SA0000CK210



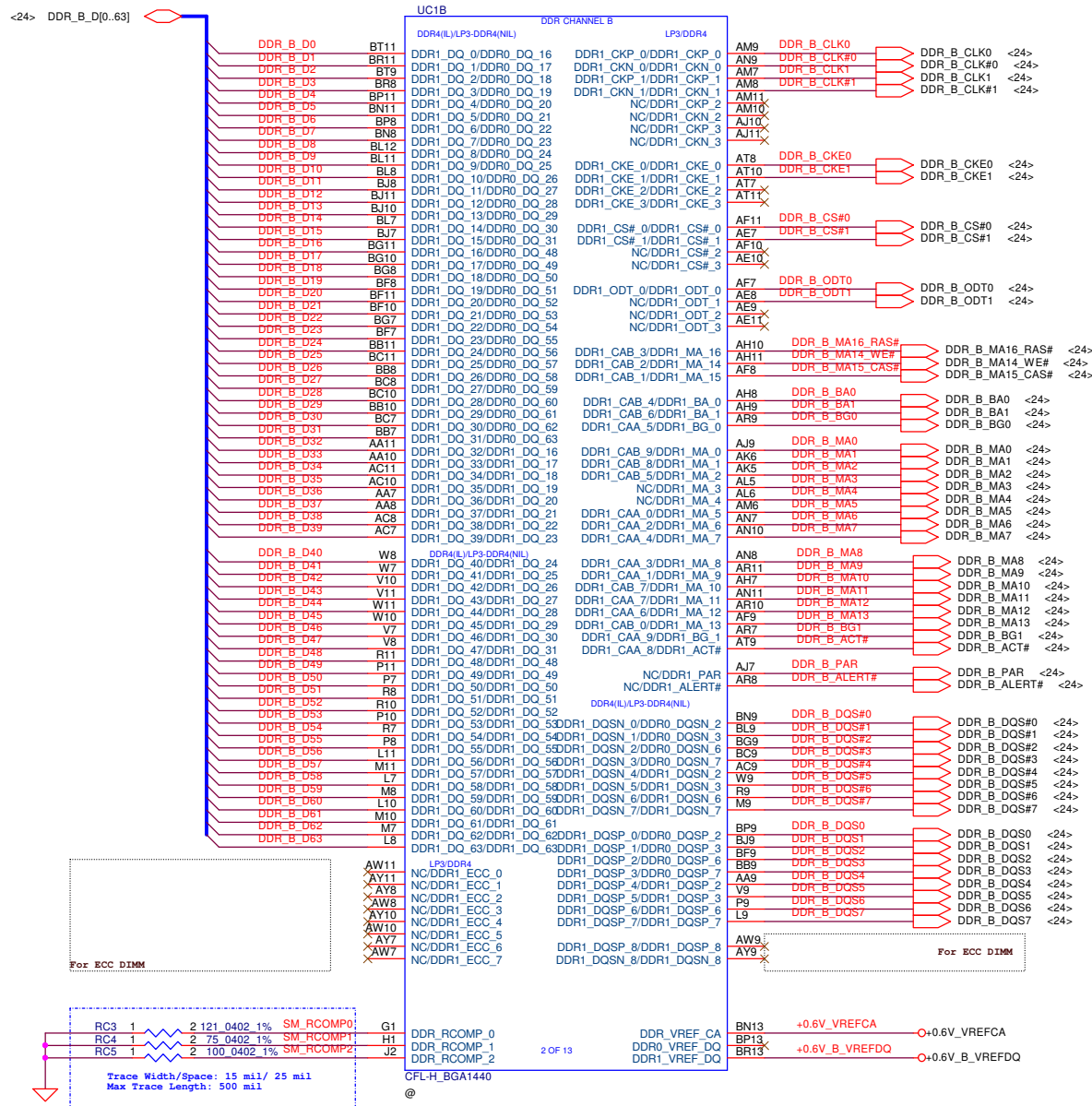
S IC N18P-G0-MP-A1 FCBGA 960P GPU ABO !
SA0000CK230



Interleaved Memory



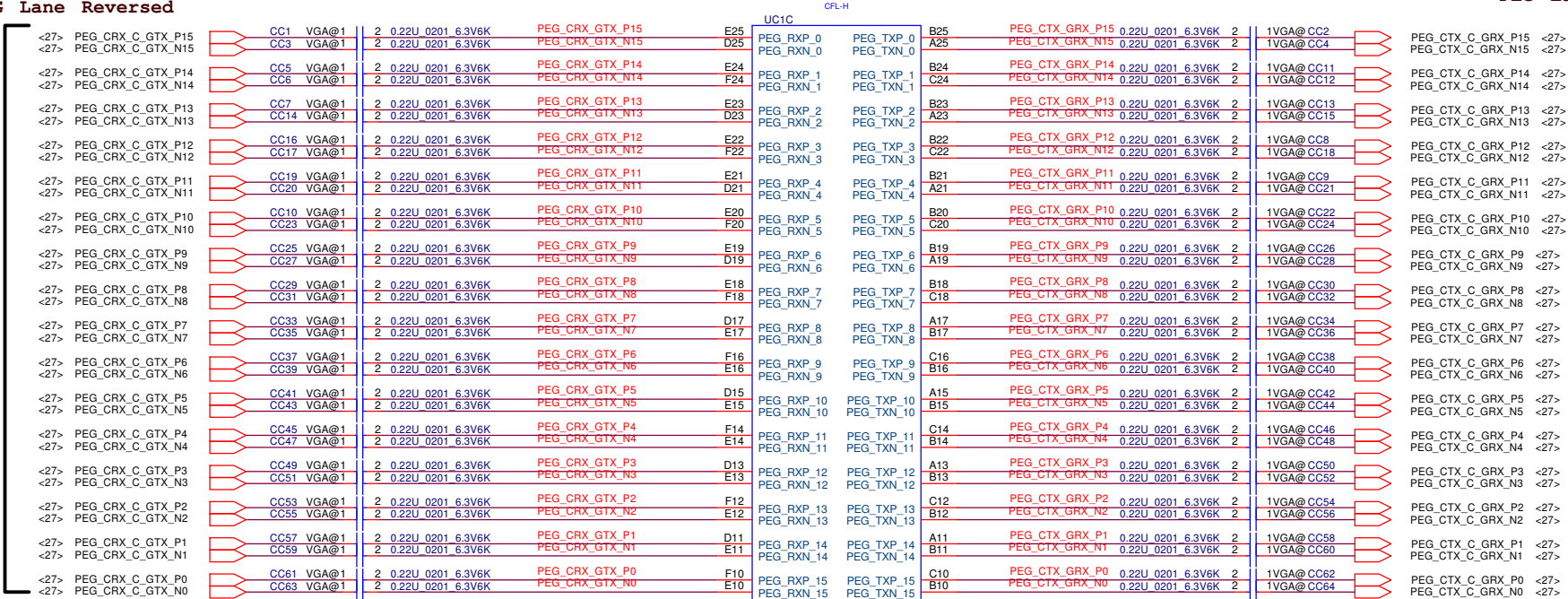
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Issued Date	2017/10/30	Deciphered Date	2018/10/30	Title	
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				Custom	1A
				Document Number EHSVF M/B LA-H501P	
				Date: Friday, February 22, 2019	Sheet 7 of 101



PEG&DMI

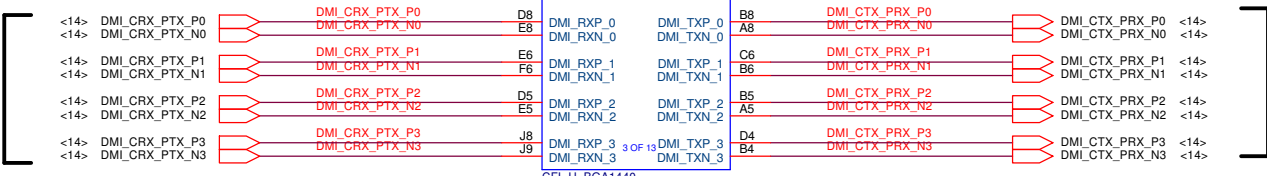
To DGPU
PEG Lane Reversed

To DGPU
PEG Lane Reversed



To PCH

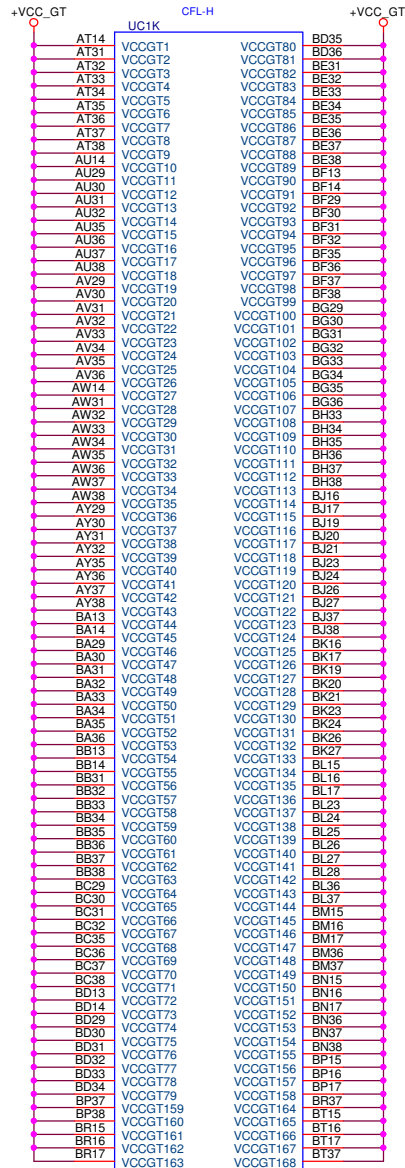
To PCH



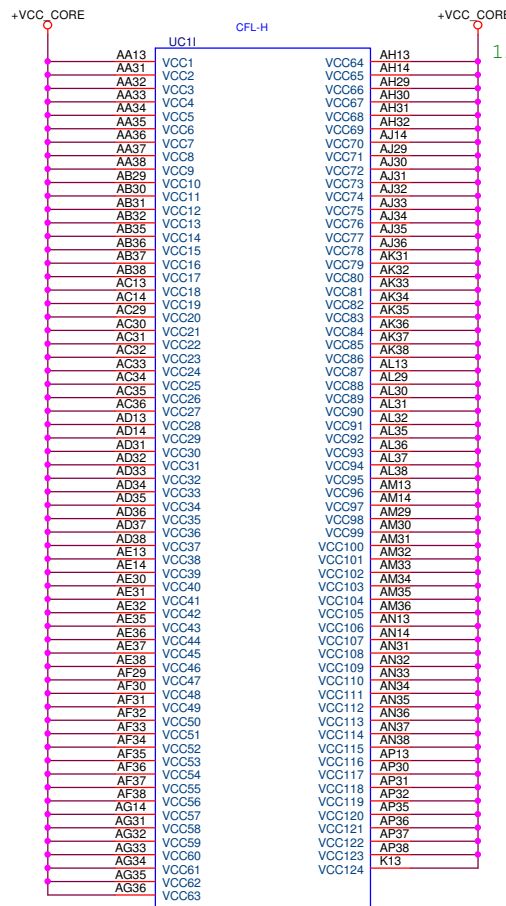
CFL-H_BGA1440



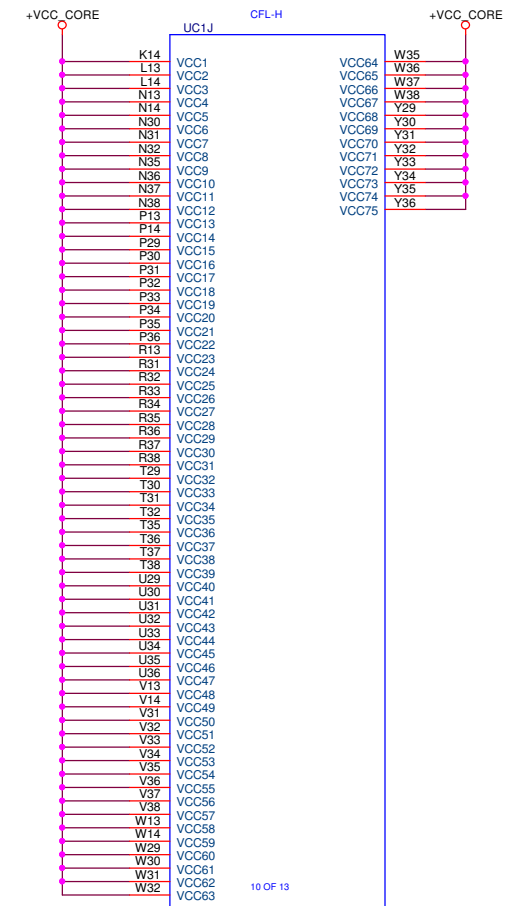
GT
32000mA (Hexa Core GT2)



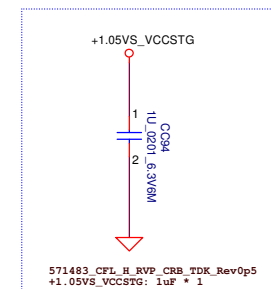
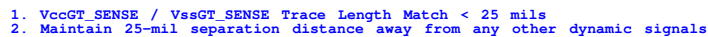
1. VccGT_SENSE / VssGT_SENSE Trace Length Match < 25 mils
2. Maintain 25-mil separation distance away from any other dynamic signals.

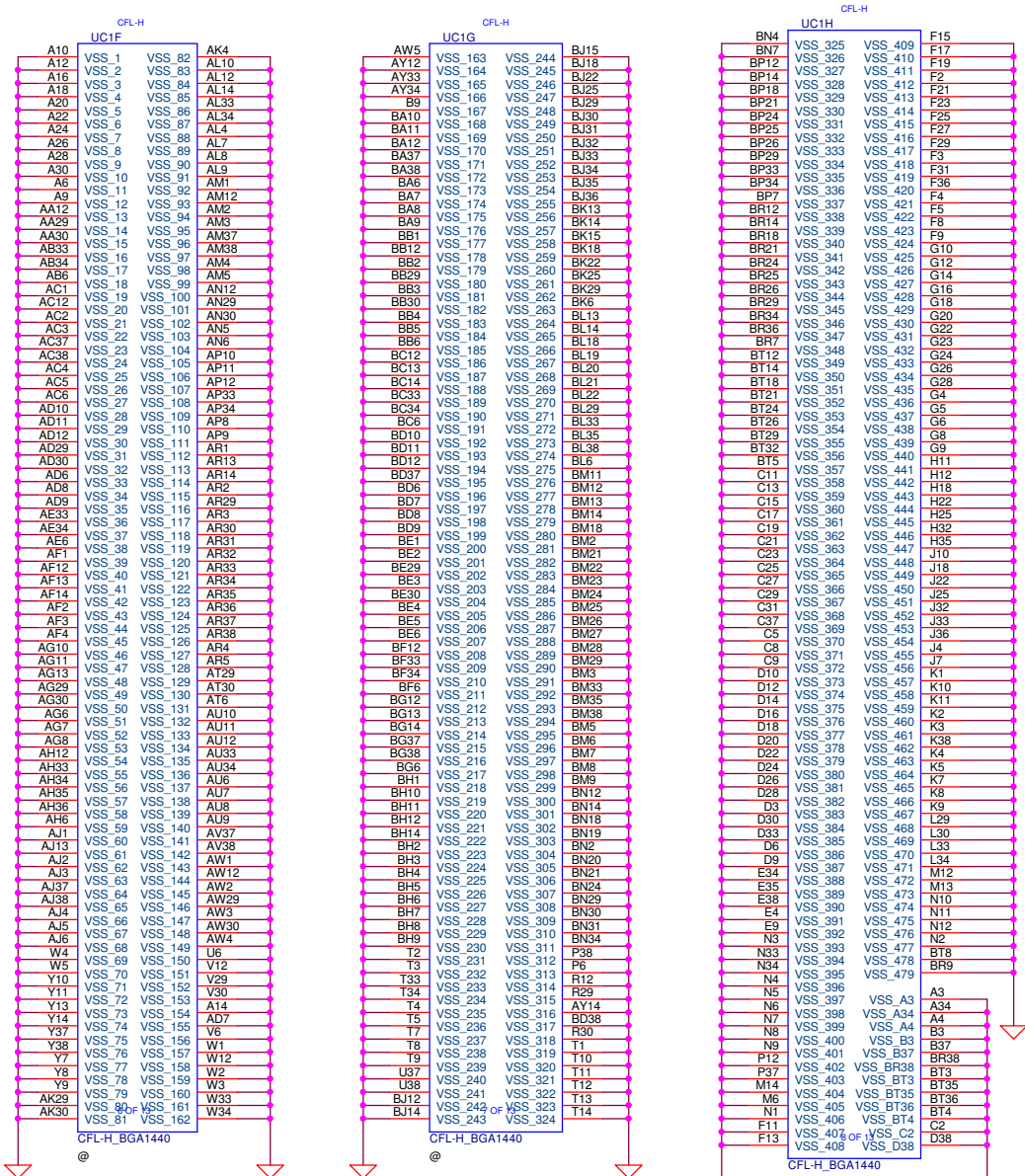
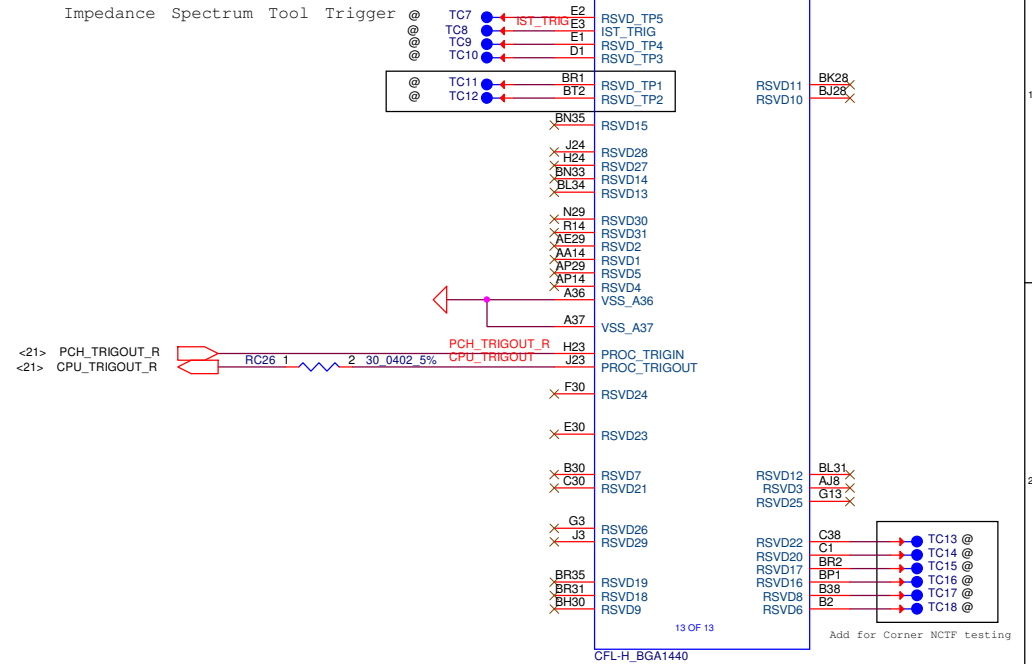


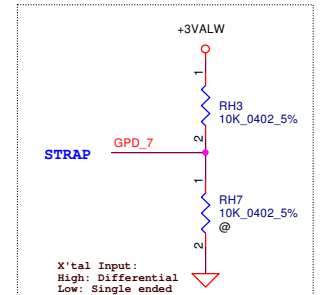
1. Vcc_SENSE/ Vss_SENSE Trace Length Match < 25 mils
2. Maintain 25-mil separation distance away from any other dynamic signals.



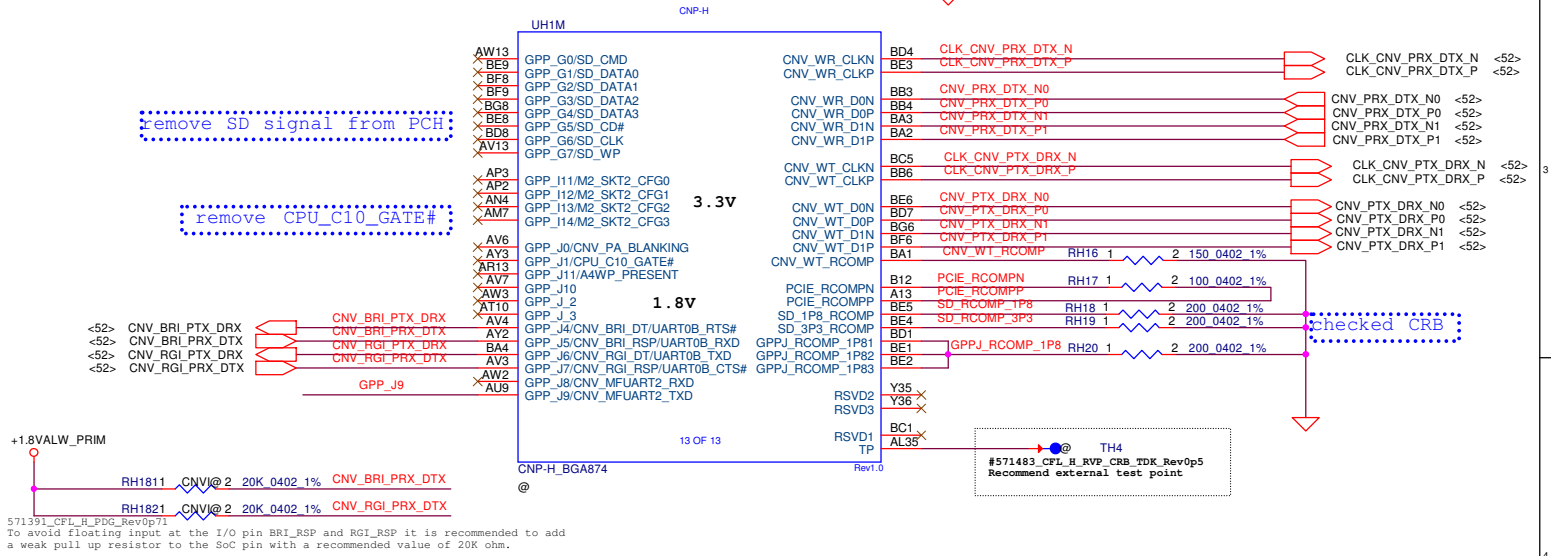
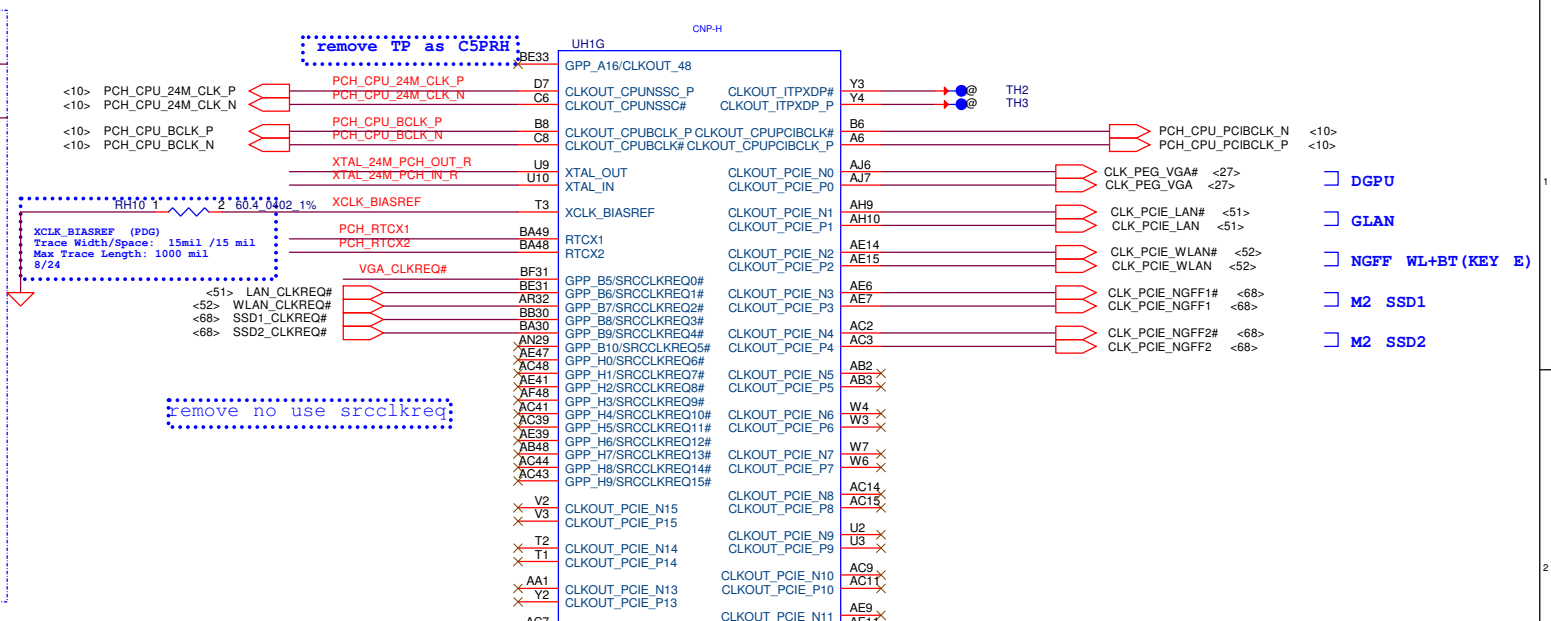
10 OF 13







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				Custom	EH5VF M/B L-H501P
				Date:	Friday, February 22, 2019



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				Custom	EH5VF M/B LA-H501P	1A
				Date:	Friday, February 22, 2019	Sheet

can remove if no use DP
08/18

remove PCH DP SCLK/SDATA:

DDP[B..F]CTRLDATA
This signal has a weak internal Pull-down.
0 = Port B-D is not detected.
1 = Port B,C,D is detected. (Default)
Notes:
1. The internal Pull-down is disabled after
PCH_PMR0K de-asserts.
2. This signal is in the primary well.

no follow naming

<27,40> HDMI_HPD_PCH

<38> EDP_HPD

<51,58> EC_PME#

CRB connect GND

<66> PCH_SPI_SI_R

<66> PCH_SPI_SO_R

<66> PCH_SPI_CLK_R

<66> PCH_SPI_CS#2

* wait confirm CG7
PDG P348 quad mode support PH1K
CRB P/U 20K
#571182 CFL_PCH_EDS_Rev1.0 recommend 100K
#571391 CFL_H_PDG_Rev071

PCH_SPI_IO2

PCH_SPI_IO3

PCH_SPI_SL_R

GPP_H15

STRAP

#571182 CFL_PCH_EDS_V1_Rev0.7
External pull-up is required. Recommend 100K if pulled
up to 3.3V or 75K if pulled up to 1.8V.
571007 CFL_MOW_Archive_WW22_2017
STUFF R on GPP_H15

PCH_SPI_CLK_R RH1951

intel critical net recommend

SPI ROM (16MByte)

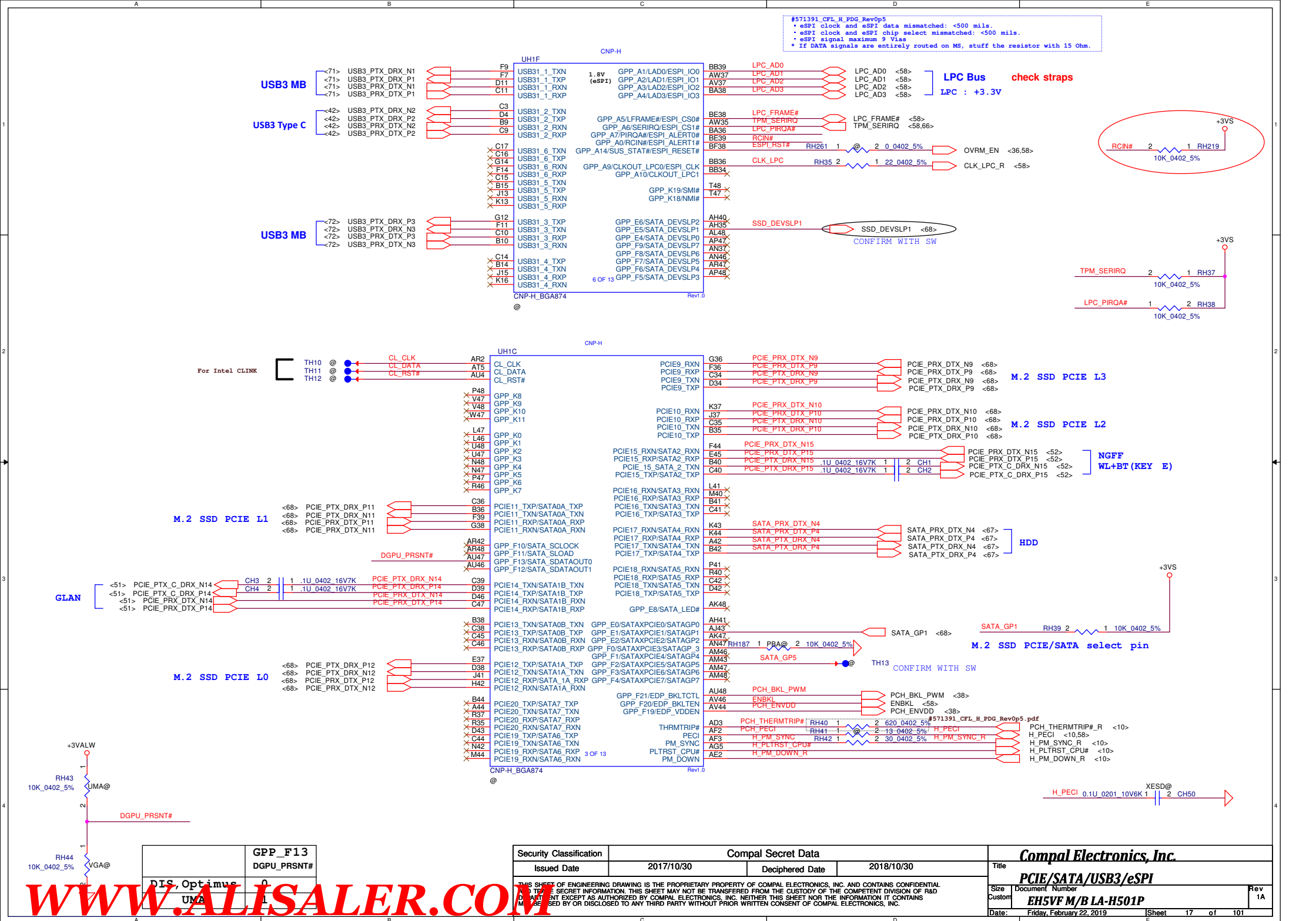
UH2
PCH_SPI_CS#0 1 /CS VCC 8
PCH_SPI_SO_0_R 2 /DO(IO1) /HOLD(IO3) CLK 7
PCH_SPI_IO2_0_R 3 /WP(IO2) DI(IO0) 6
4 GND 5
W25Q128FVSIQ_S08
XMC P/N: SA0000B8400

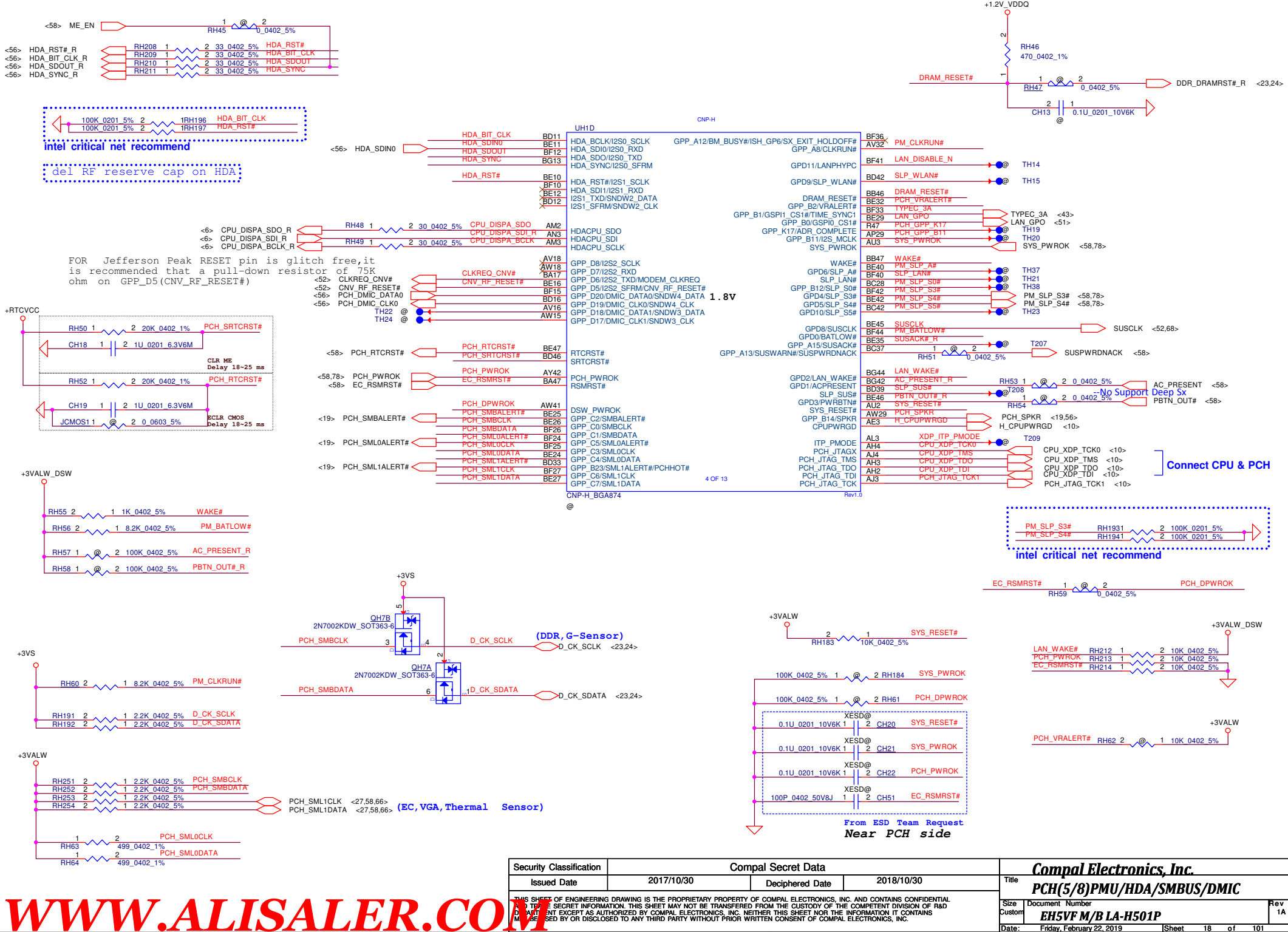
PCH_SPI_CLK_0_R 1 XEMI@ 2
RH33 0_0402_5% CH12 68P_0402_50V8J

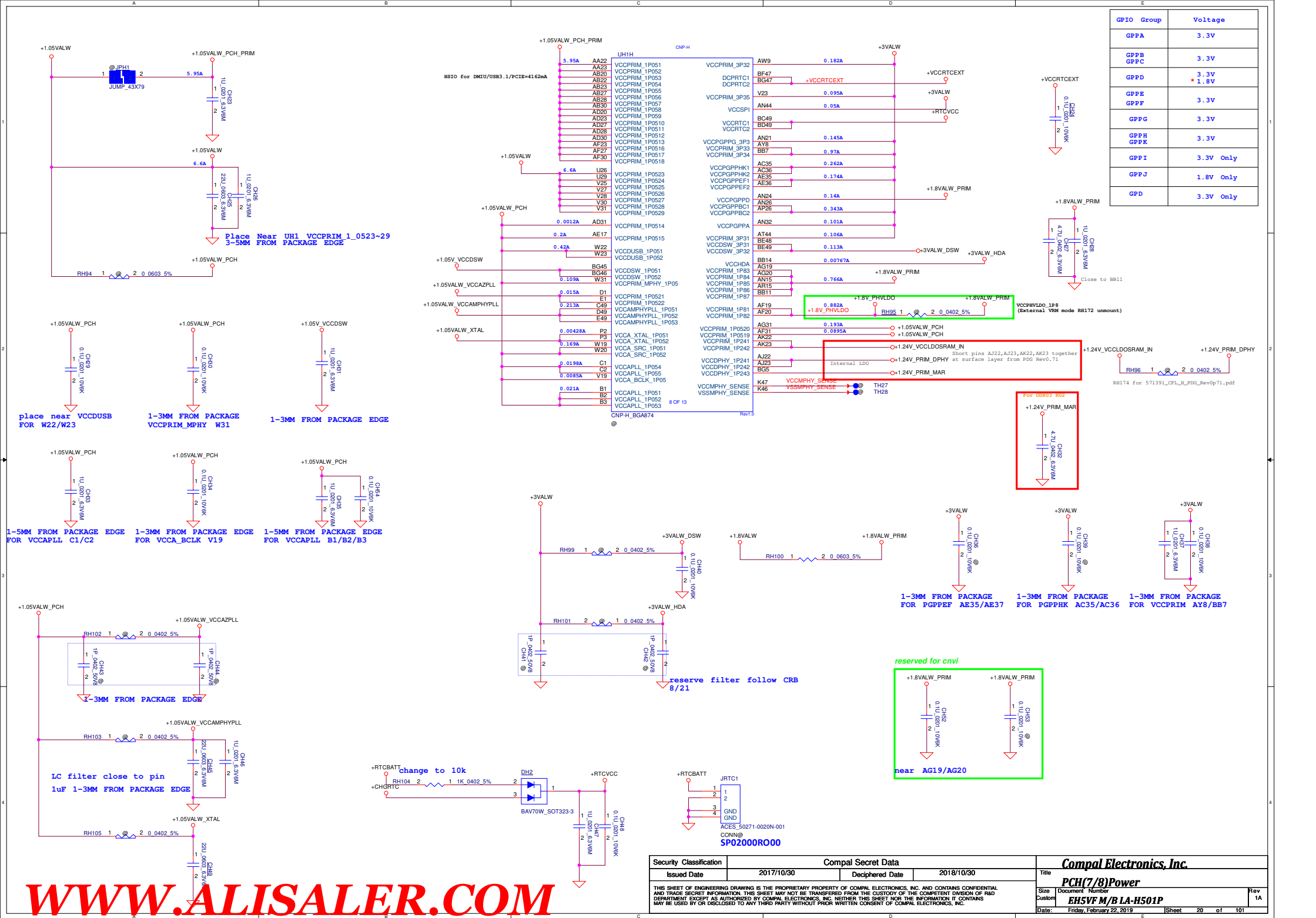
PCH_SPI_SL_0_R RH107 1 2 33_0402_1% PCH_SPI_SL_R
PCH_SPI_SO_0_R RH108 1 2 33_0402_1% PCH_SPI_SO_R
PCH_SPI_IO3_0_R RH109 1 2 33_0402_1% PCH_SPI_IO3
PCH_SPI_CLK_0_R RH110 1 2 33_0402_1% PCH_SPI_CLK_R
PCH_SPI_IO2_0_R RH111 1 2 33_0402_1% PCH_SPI_IO2

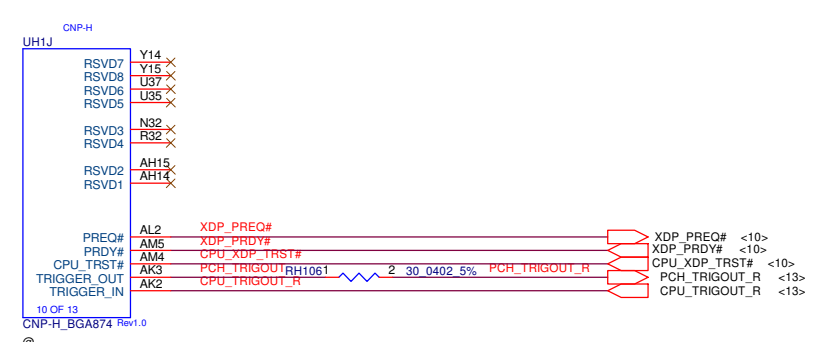
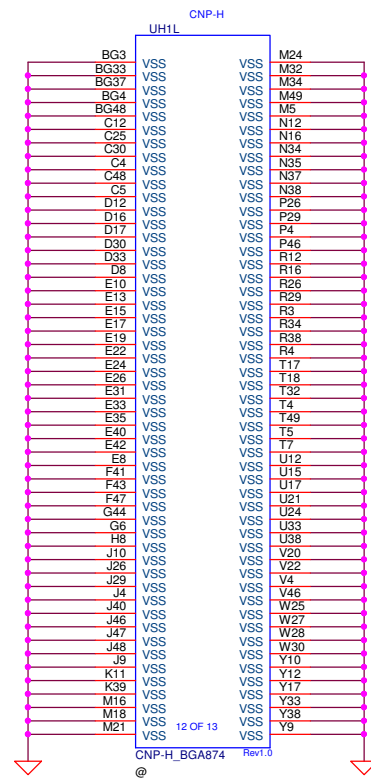
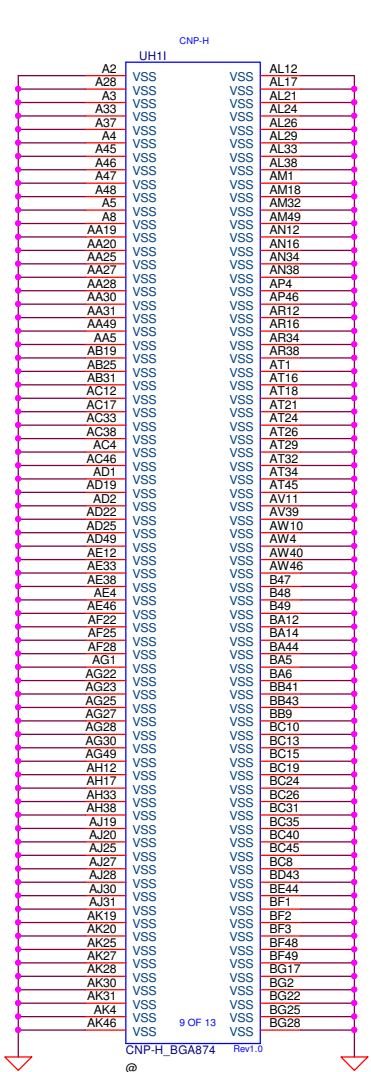
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				PCH(3/8)DDC/SPI	
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		Custom		EHSVF M/B LA-H501P	1A
		Date:		Fri, Feb 22, 2019	Sheet 16 of 101

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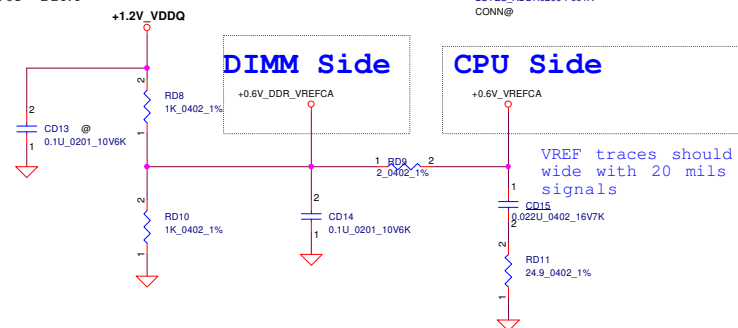
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								PCH(8/8)GND/RSVD			
Size		Document Number						Rev			
Custom		EH5VF M/B LA-H501P						1A			
Date:		Friday, February 22, 2019						Sheet 21 of 101			

Reserve Page

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				EH5VF M/B LA-H501P	
				Date:	Friday, February 22, 2019
				Sheet	22 of 101
				Rev	1A

Interleaved Memory

Layout Note:
Place near JDIMM1



VREF traces should be at least 20 mils wide with 20 mils spacing to other signals

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				Date: Friday, February 23, 2019	Sheet 23 of 101

Reserve Page

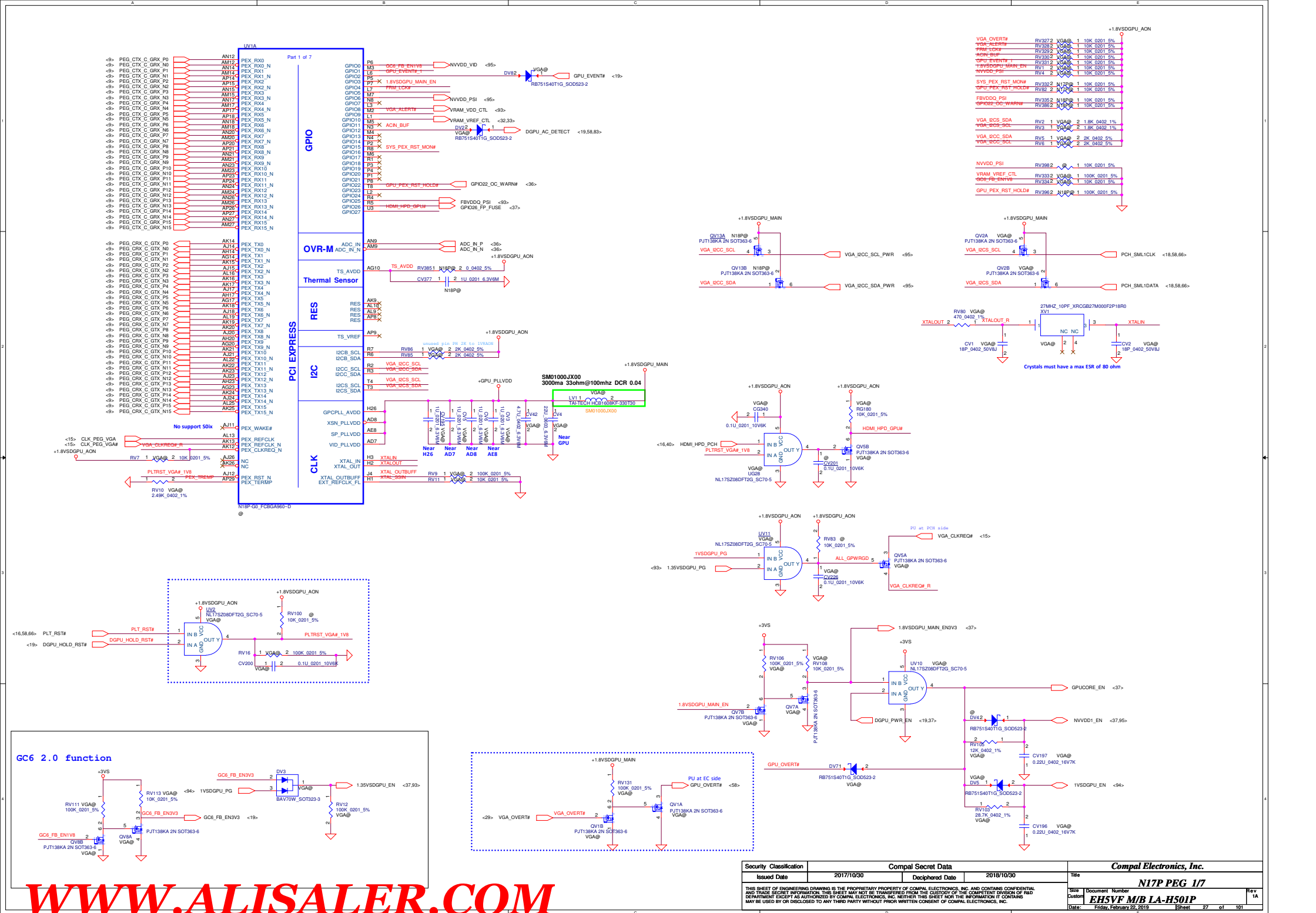
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				Date:	Friday, February 22, 2019
				Sheet	25 of 101
				Rev	1A

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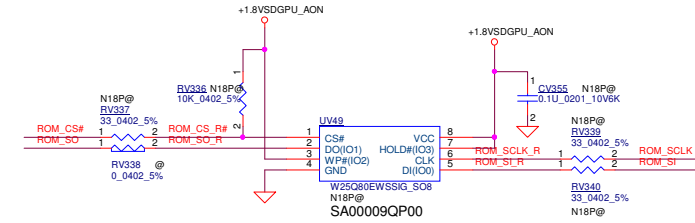
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				Sheet	26 of 101
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Memory Density	Allowed Memory Configuration	FBVDD/Q	Vendor	Manufacturer Part Number	Die Revision	Strap	Memory Speed Grade	Date Code Alert	Qual Plan	Status
8 Gb	256Mx32	1.35V and 1.5V ⁶	Samssung	K4G80325FB-HC28	B-die	0x0	7 Gbps	11/A	Full	Production ready ⁷
			Samssung	K4G80325FB-HC25	B-die	0x0	8 Gbps	11/A	11/A	Substitution allowed with waiver ⁸
			Micron	MT51J256M32HF-70:A	A-die	0x1	7 Gbps	11/A	Full	Production ready
			Micron	MT51J256M32HF-80:A	A-die	0x1	8 Gbps	11/A	11/A	Substitution allowed with waiver ⁹
			Hynix	H5GCRH24AJR-R0C	M-die	0x2	7 Gbps	11/A	Full	Post production ready
			Hynix	H5GQRH24AJR-R4C	M-die	0x2	8 Gbps	11/A	11/A	Substitution allowed with waiver ⁹
			Micron	MT51J256M32HF-70:B	B-die	0x4	7 Gbps	11/A	Full	Post production ready
			Micron	MT51J256M32HF-80:B	B-die	0x4	8 Gbps	11/A	11/A	Substitution allowed with waiver ⁹
			Hynix	H5GCRH24AJR-R0C	A-die	0x5	7 Gbps	11/A	Full	Post production ready
			Hynix	H5GQRH24AJR-R2C	A-die	0x5	8 Gbps	11/A	11/A	Substitution allowed with waiver ⁹

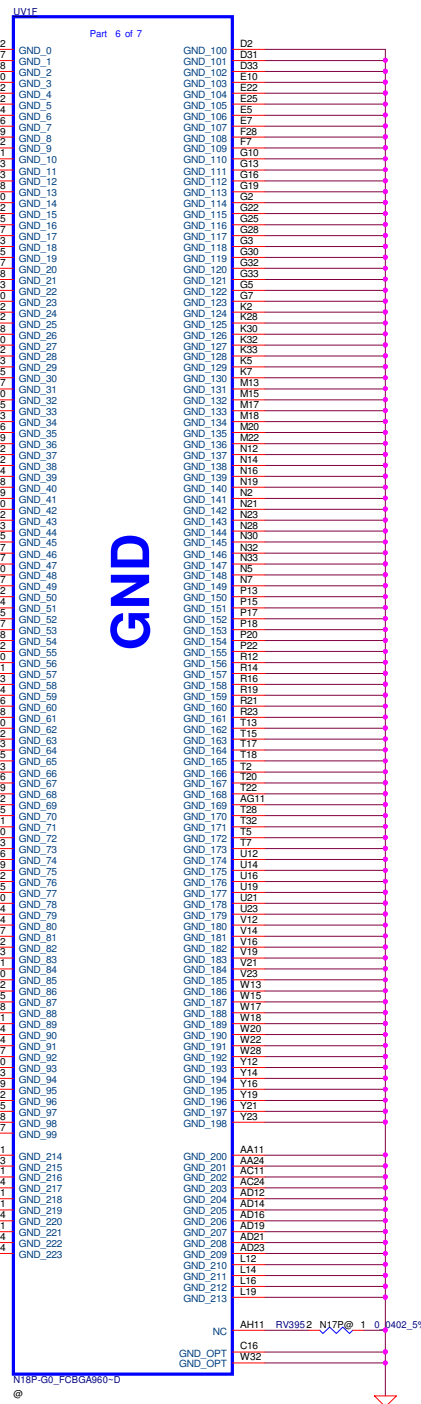
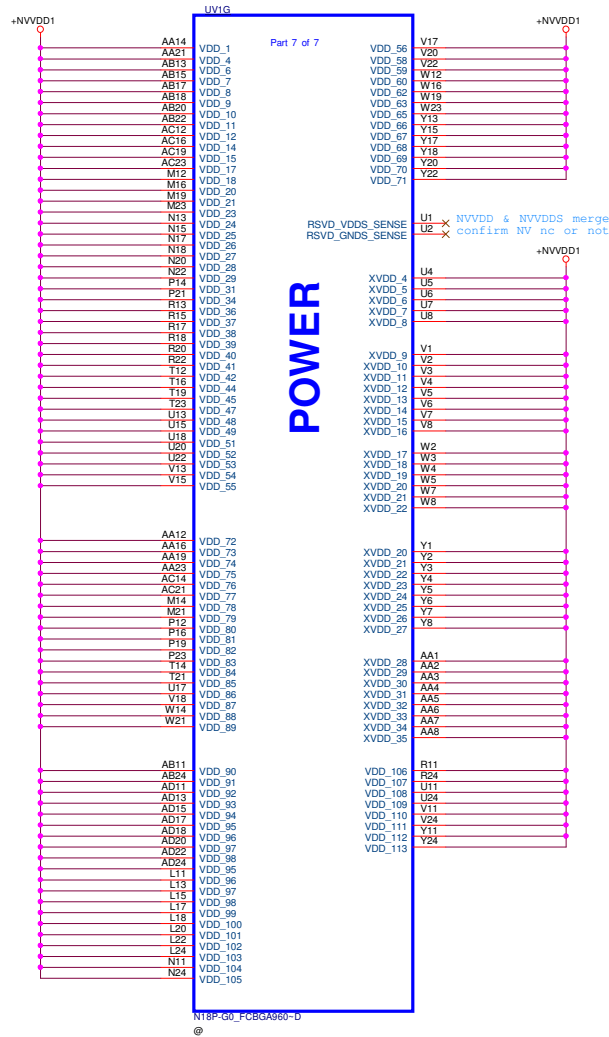
Memory Density	Allowed Memory Configuration	FBVDD/Q	Vendor	Manufacturer Part Number	Die Revision	Strap	Memory Speed Grade	Date Code Alert	Qual Plan	Status
8 Gb	256Mx32	1.35 V and 1.55V ²	Micron	MT15J256M32HF-80-B	B-die	0x1	8 Gbps	H/A	Full	Production candidate
			Hynix	H5GCBH2-4AJR-R2C	A-die	0x2	8 Gbps	H/A	Full	Production candidate
			Samsung	K4G80325FC-HC25	C-die	0x0	8 Gbps	H/A	Full	Production candidate

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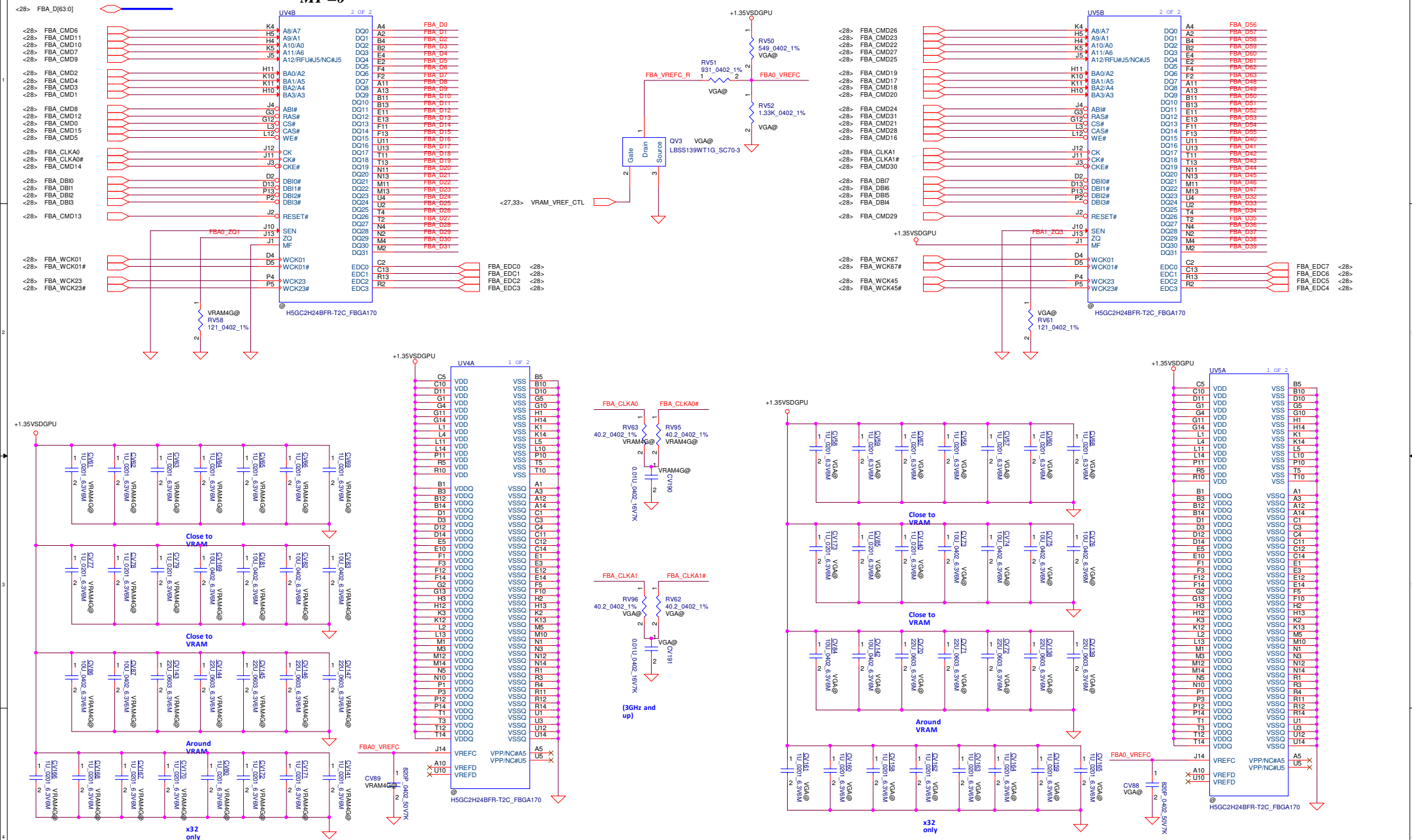
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1uF*5/4.7uF*5 (under GPU)
330uF*1/22uF*3/10uF*2/4.7uF*2



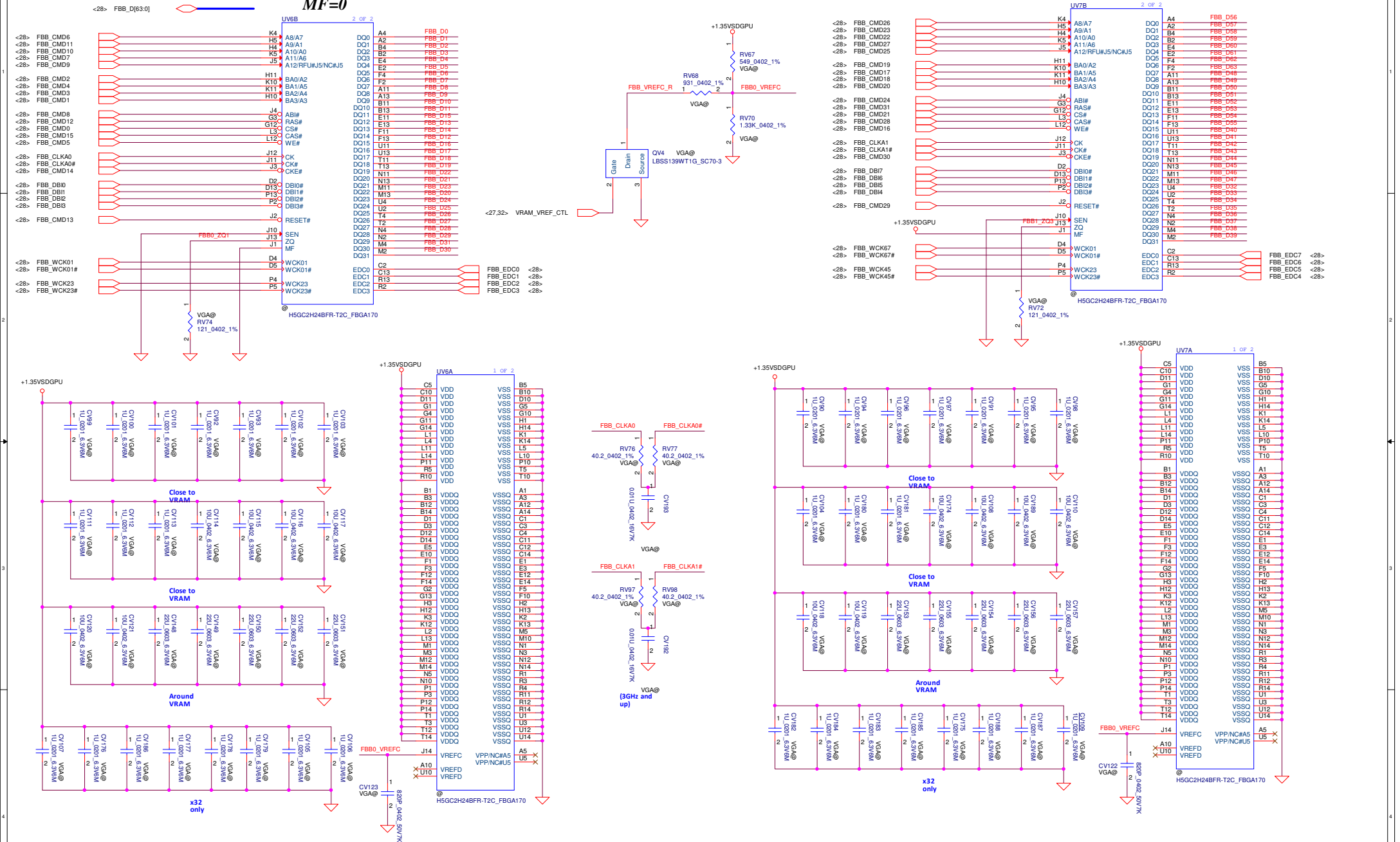
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					Date:	Friday, February 22, 2019	Sheet	31	of	101

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				Date:	Friday, February 22, 2019
				Sheet	32 of 101

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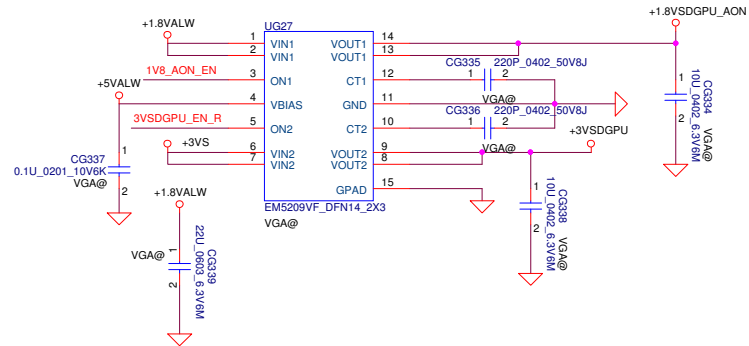
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				Sheet	34 of 101
				Rev	1A

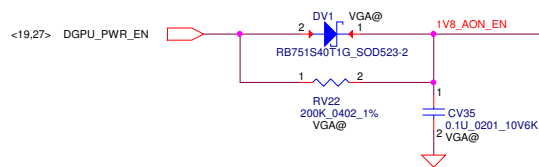
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				Sheet	35 of 101
				Rev	1A

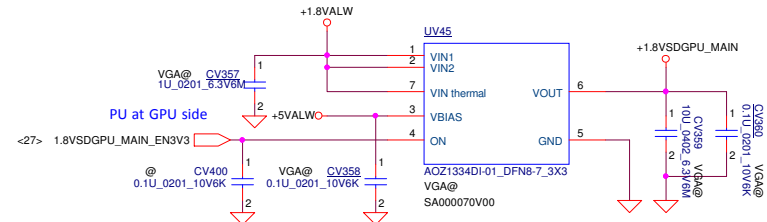
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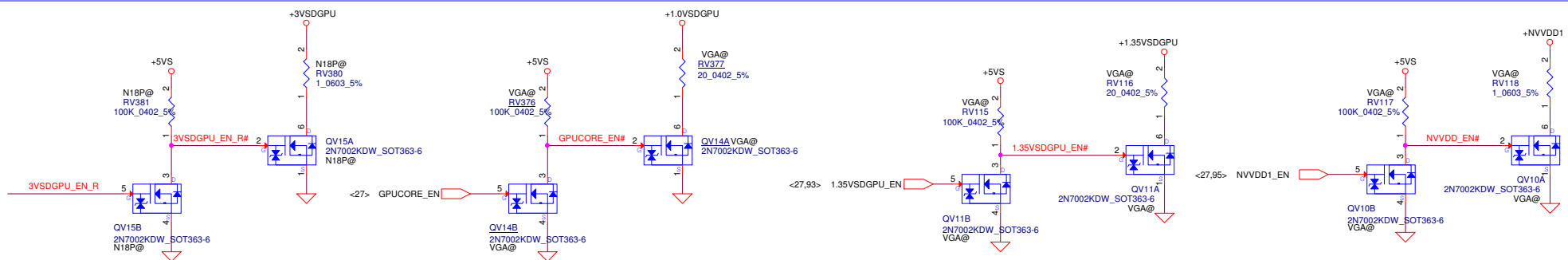
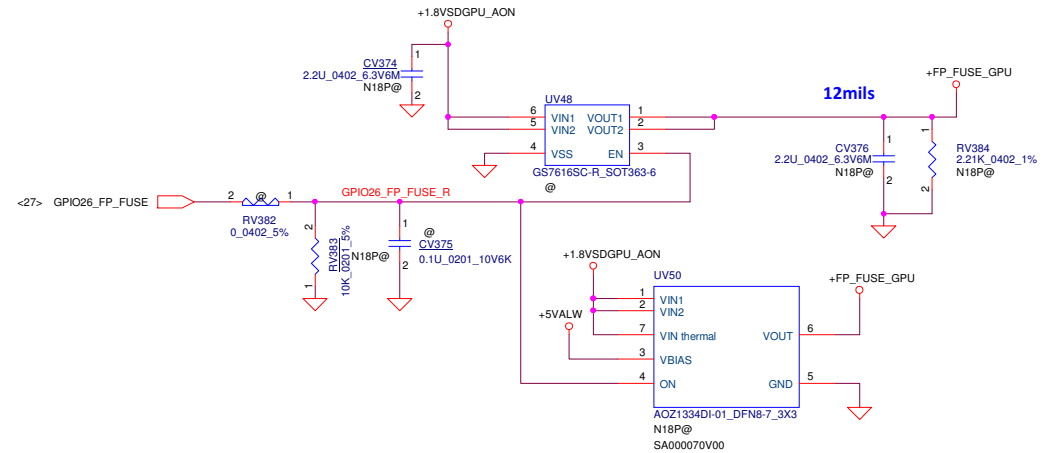
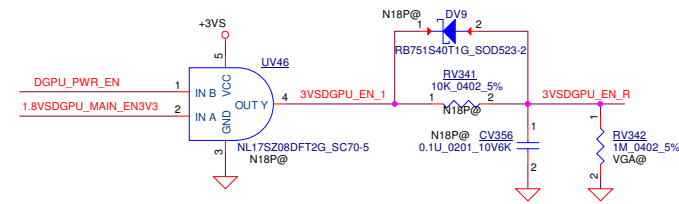
For Power down sequence



+1.8V_MAIN

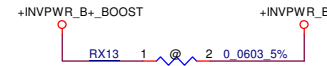
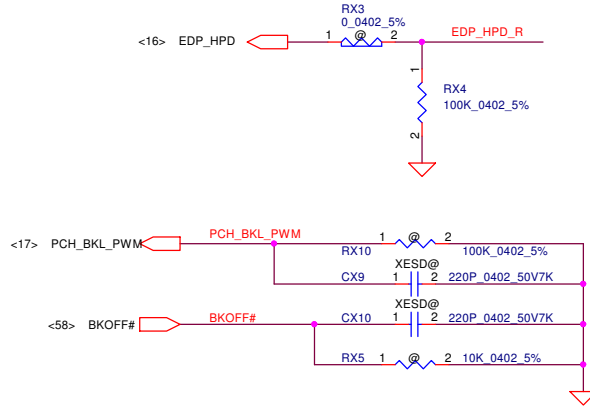
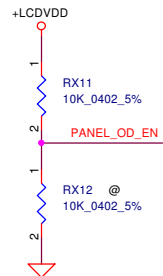
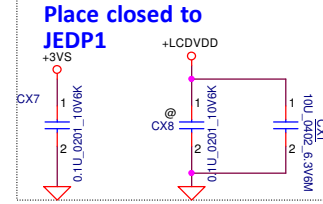
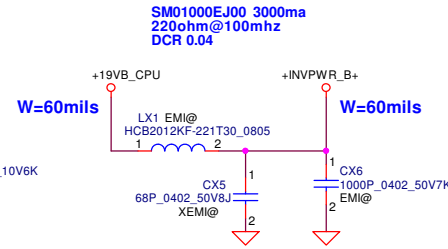
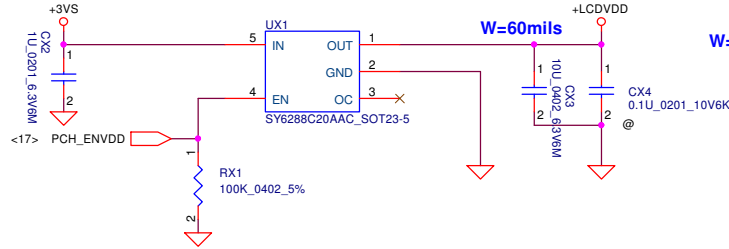


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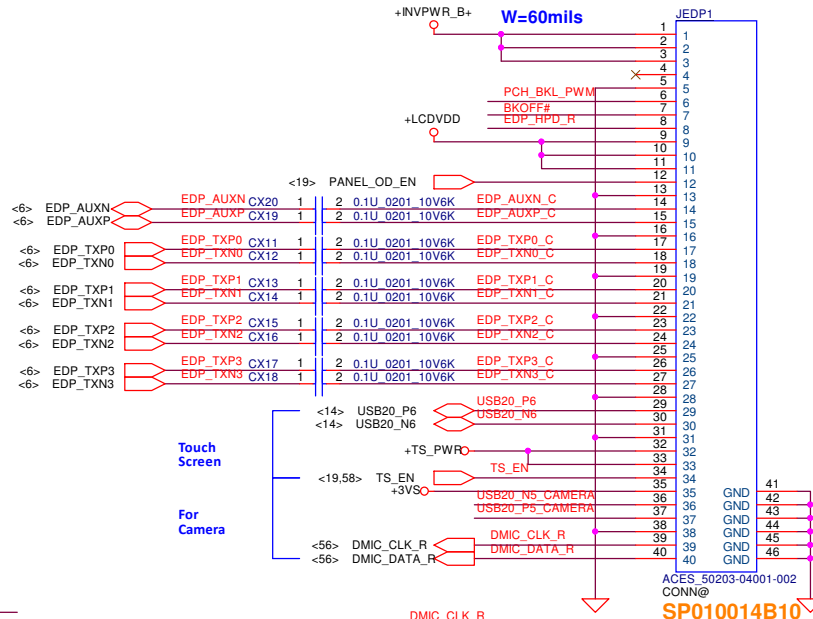


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				Sheet	37 of 101
				Rev	1A

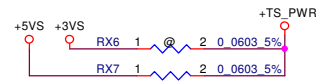
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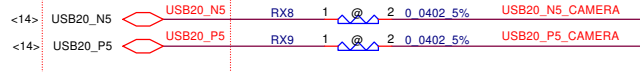
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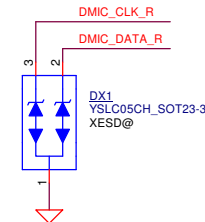
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Camera



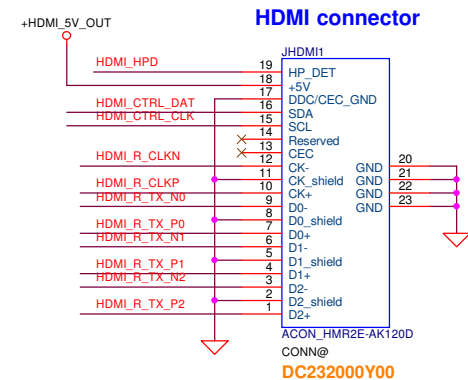
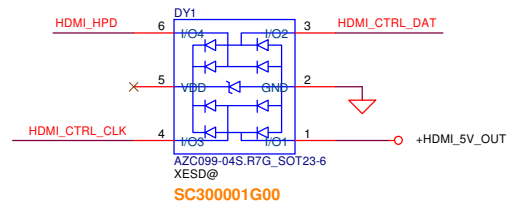
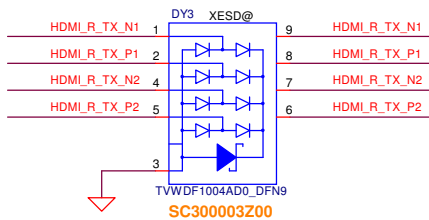
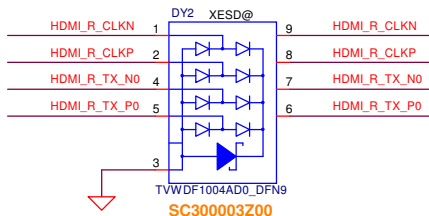
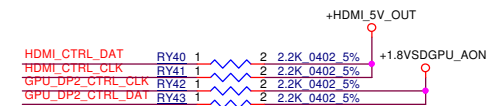
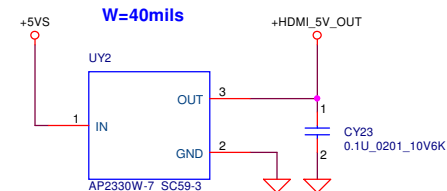
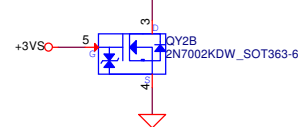
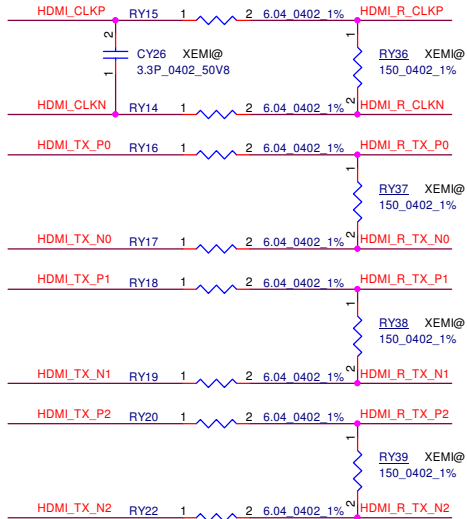
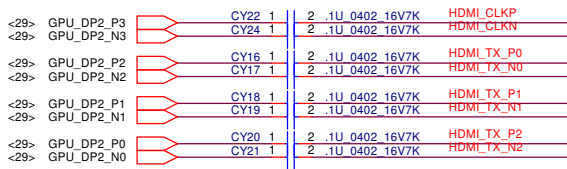
Touch Screen
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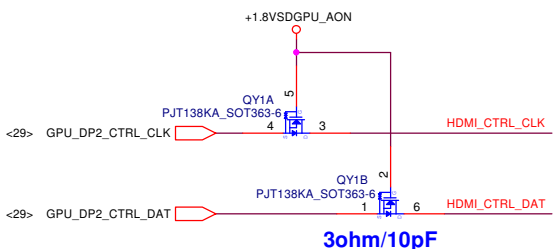
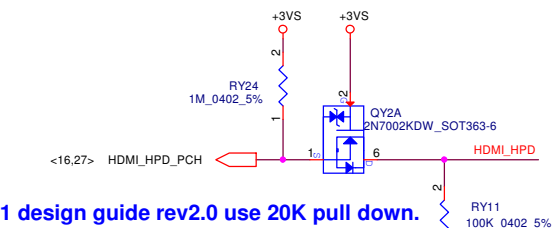
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				Date:	Friday, February 22, 2019
				Sheet	38 of 101
				Rev	1A

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RY11 design guide rev2.0 use 20K pull down.



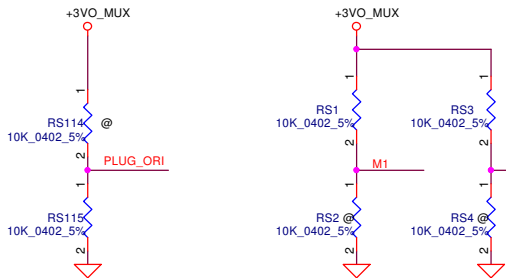
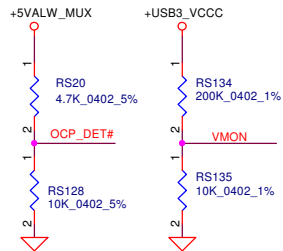
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										Sheet 40 of 101	

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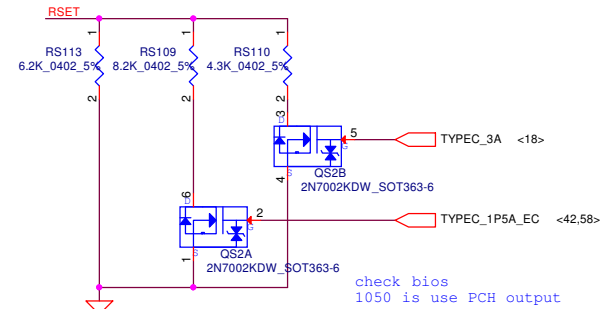
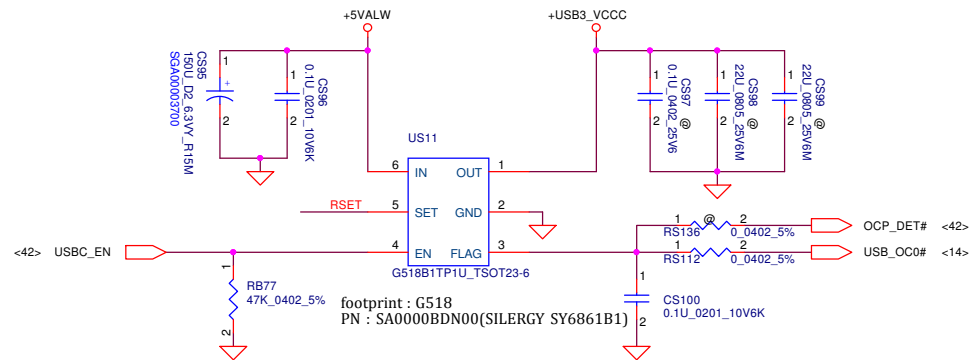
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				Sheet	41 of 101
				Rev	1A

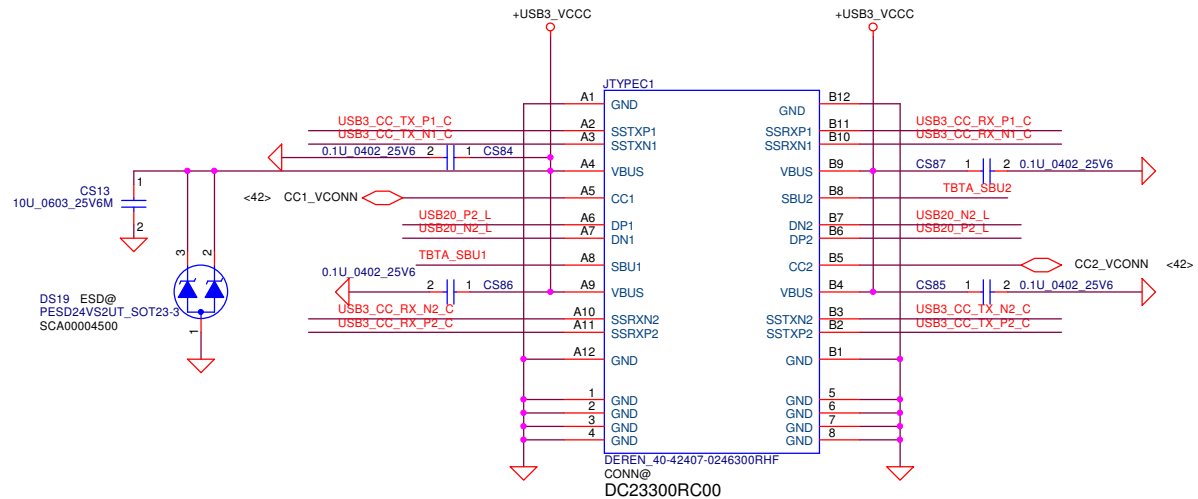
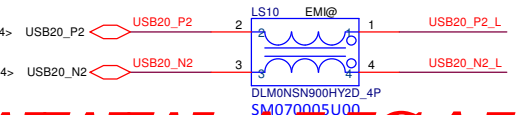
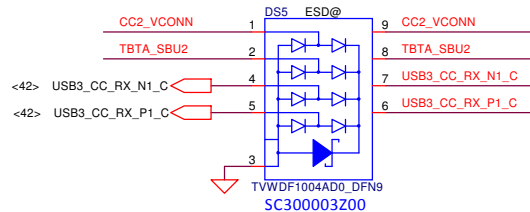
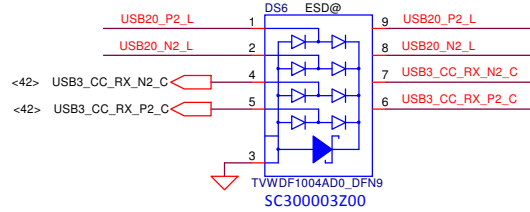
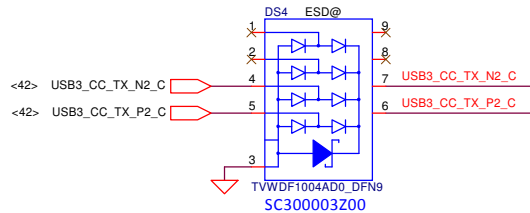
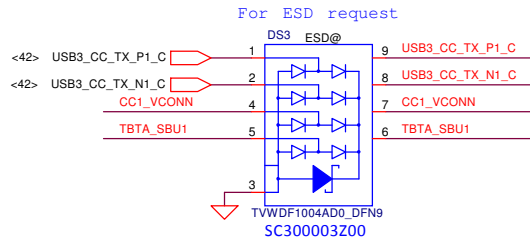


RTS5441 M0 truth table by 2018 BIOS spec			
TYPEC_1P5A_EC	MODE	limit point	Condition
H	3A	3.5A	AC mode or Battery >30%
L	1.5A	1.92A	Battery <30% when DC mode

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				Size	Document	Number	Rev
				Custom		EHSVF M/B LA-H501P	1A
Date:		Friday, February 22, 2019		Sheet	42	of	101



G518 MOS Current Limit				
GPP_B1 (TYPE3A)	GPP_B4 (TYPE3A)	RSET(kΩ)	MODE	limit point
L	L	6.2	0.9A	1.09A
L	H	3.53	1.5A	1.92A
H	L	2.54	2A	2.67A
*H	H	1.94	3A	3.5A



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Deciphered Date				2018/07/20				CC+USB TYPE C		
Size				Document Number				EH5VF M/B LA-H501P		
Date				Friday, February 22, 2019				Sheet 43 of 101		

Reserve Page

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				Size	Document Number
				EH5VF M/B LA-H501P	
Date:		Friday, February 22, 2019		Sheet	44 of 101
Rev		1A			

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				Rev	
				1A	
Date:		Friday, February 22, 2019		Sheet	45 of 101

Reserve Page

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				EH5VF M/B LA-H501P	
				Date:	Friday, February 22, 2019
				Sheet	46 of 101
				Rev	1A

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				EH5VF M/B LA-H501P	
				Date:	Friday, February 22, 2019
				Sheet	47 of 101
				Rev	1A

Reserve Page

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Date:		Friday, February 22, 2019		Sheet	48 of 101

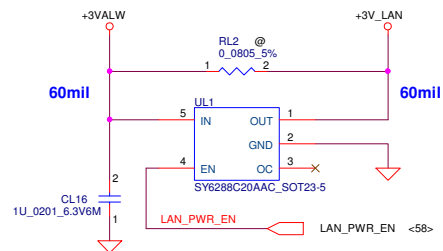
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				EH5VF M/B LA-H501P	
				Date:	Friday, February 22, 2019
				Sheet	49 of 101
				Rev	1A

Reserve Page

Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2017/11/23	Deciphered Date	2017/12/31	Title	N18E-GDDR6 D
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				EH5VF M/B LA-H501P	
				Date:	Friday, February 22, 2019
				Sheet	50 of 101
				Rev	1A

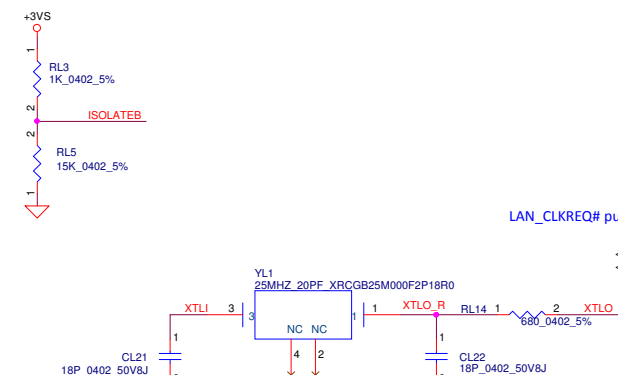
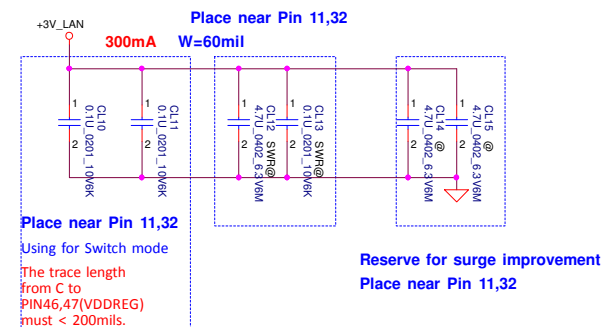
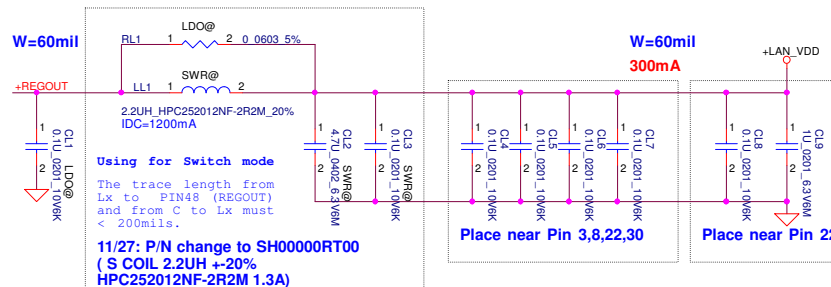
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RTL8111H LDO mode
RTL8118ASA SWR mode
```



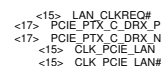
```

From EC
High active.
EN threshold voltage min:1.2V
typ:1.6V max:2.0V
Current limit threshold 1.5~2.8A
+3V_LAN Rising time must >0.5ms

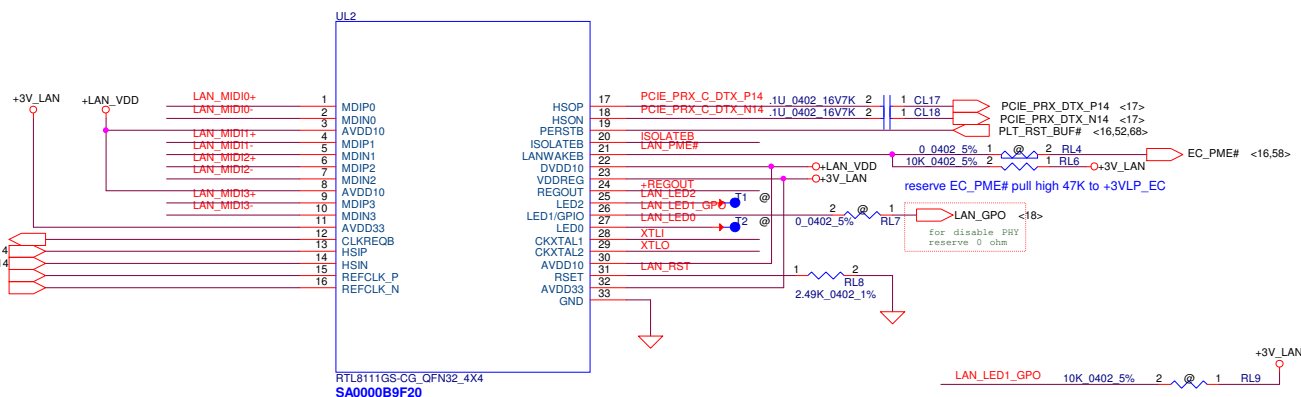
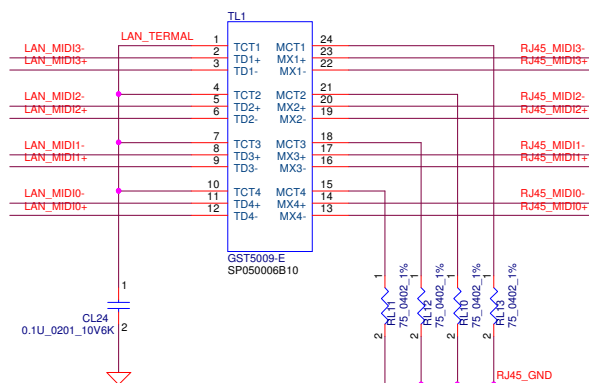
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LAN CLKREQ# pull up at PCH side

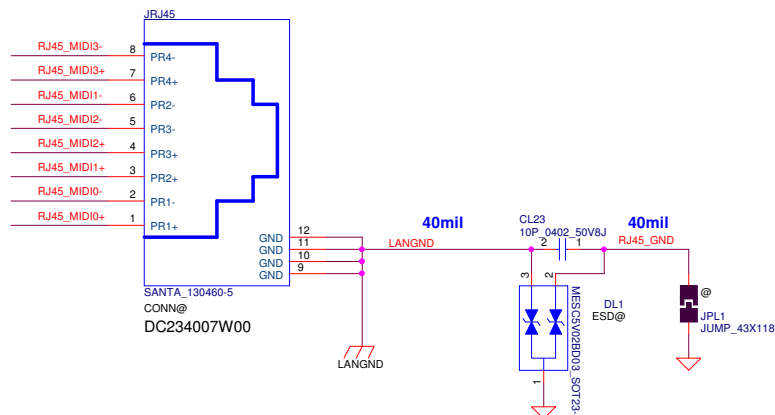


P/N: SJ10000UP00 (S CRYSTAL 25MHZ 10PF XRCGB25M000F2P34R0)



SA0000B9F20, S IC RTL8118ASA-CG QFN 32P E-LAN CTRL

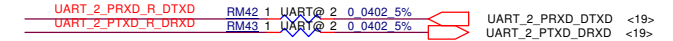
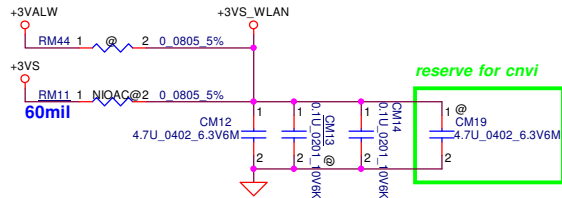
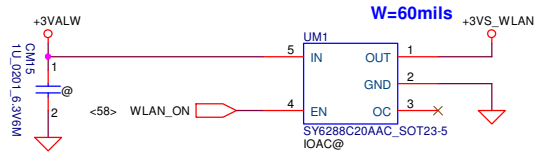
LAN Connector



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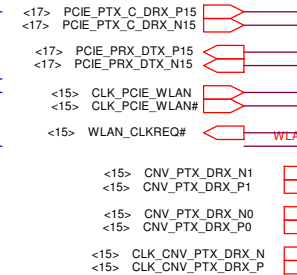
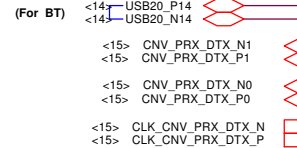
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				Size	Document Number		Rev	
				Custom	EH5VF M/B LA-H501P		1A	
				Date: Friday, February 22, 2019		Sheet	51	of

Wireless LAN



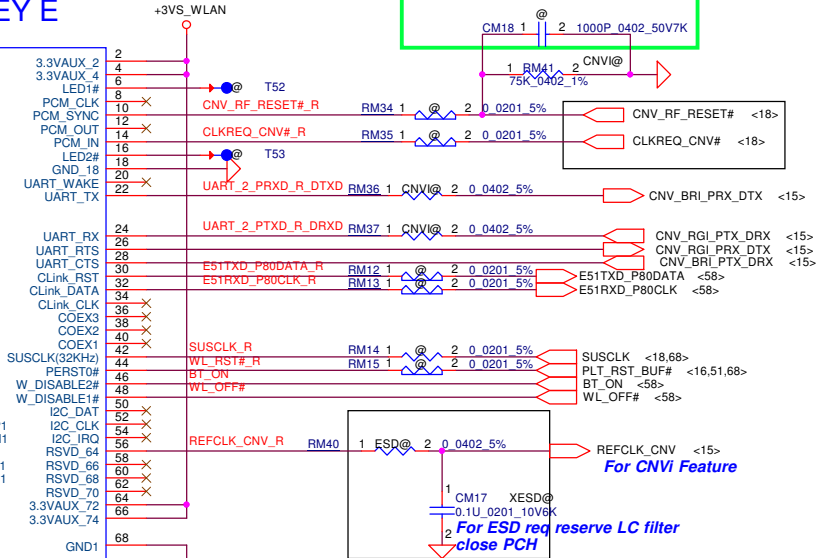
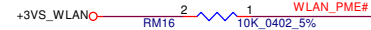
Co-layout with CNVi for SW debug

KEY E



(link to PICE Port 3)
PCIE X1

(From PCH CLKOUT2)
PCIE CLK



reserve 1000p for cnvi

For CNVi Feature

For ESD req reserve LC filter
close PCH

reserve for BT_ON OD pull high (1.0)



NGFF WL+BT (KEY E)

74	3.3V	GND	75
72	3.3V	RESERVED/REFCLKN1	73
70	UM_Power_SRC(GPIQ/PEWake#	RESERVED/REFCLKP1	71
68	UM_Power_SINK/CLKREQ2#	GND	69
66	UM_SWP/PERST#	Reserved/PERn1	67
64	RESERVED	Reserved/PERp1	65
62	ALERT# (IO/Q3.3)	Reserved/PTEn1	61
60	I2C CLK (IO/Q3.3)	Reserved/PTCn1	59
58	I2C DATA (IO/Q3.3)	Reserved/PTCp1	57
56	WL_DISABLE1# (IO/Q3.3V)	PEWake0# (IO/Q3.3V)	55
54	Reserved/W_DISABLE2# (IO/Q3.3V)	CLKREQ0# (IO/Q3.3V)	53
52	PERST0N (IO/Q3.3V)	GND	51
50	SUSCLK(32KHz) (IO/Q3.3V)	REFCLKN0	49
48	COEX1 (IO/Q1.8V)	REFCLKP0	47
46	COEX3 (IO/Q1.8V)	GND	45
44	COEX2 (IO/Q1.8V)	PERn0	43
42	VENDOR DEFINED	PERp0	41
40	VENDOR DEFINED	GND	39
38	VENDOR DEFINED	PTEn0	37
36	UART RTS (IO/Q1.8V)	PETp0	35
34	UART CTS (IO/Q1.8V)	GND	33
32	UART TX (IO/Q1.8V)	SDIO Reserve (IO/Q1.8V)	23
30	UART RX (IO/Q1.8V)	SDIO Wake0# (IO/Q1.8V)	21
28	UART Wake0# (IO/Q3.3V)	SDIO DATA (IO/Q1.8V)	19
26	GND	SDIO DATA (IO/Q1.8V)	17
24	LED2# (I/O)	SDIO DATA (IO/Q1.8V)	15
22	PCM_OUT/IS_SD_OUT (IO/Q1.8V)	SDIO DATA (IO/Q1.8V)	13
20	PCM_IN/IS_SD_IN (IO/Q1.8V)	SDIO CMD (IO/Q1.8V)	11
18	PCM_SYNC/IS_WS (IO/Q1.8V)	SDIO CLK (IO/Q1.8V)	9
16	PCM_CLK/IS_SCK (IO/Q1.8V)	GND	7
14	LED1# (I/O)	USA_2#	5
12	GND	USA_1#	3
10	GND	USA_0#	1

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				Custom	EH5VF M/B LA-H501P
				Date	Friday, February 22, 2019
				Sheet	52 of 101
				Rev	1A

Reserve Page

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				EH5VF M/B LA-H501P	
				Date:	Friday, February 22, 2019
				Sheet	53 of 101
				Rev	1A

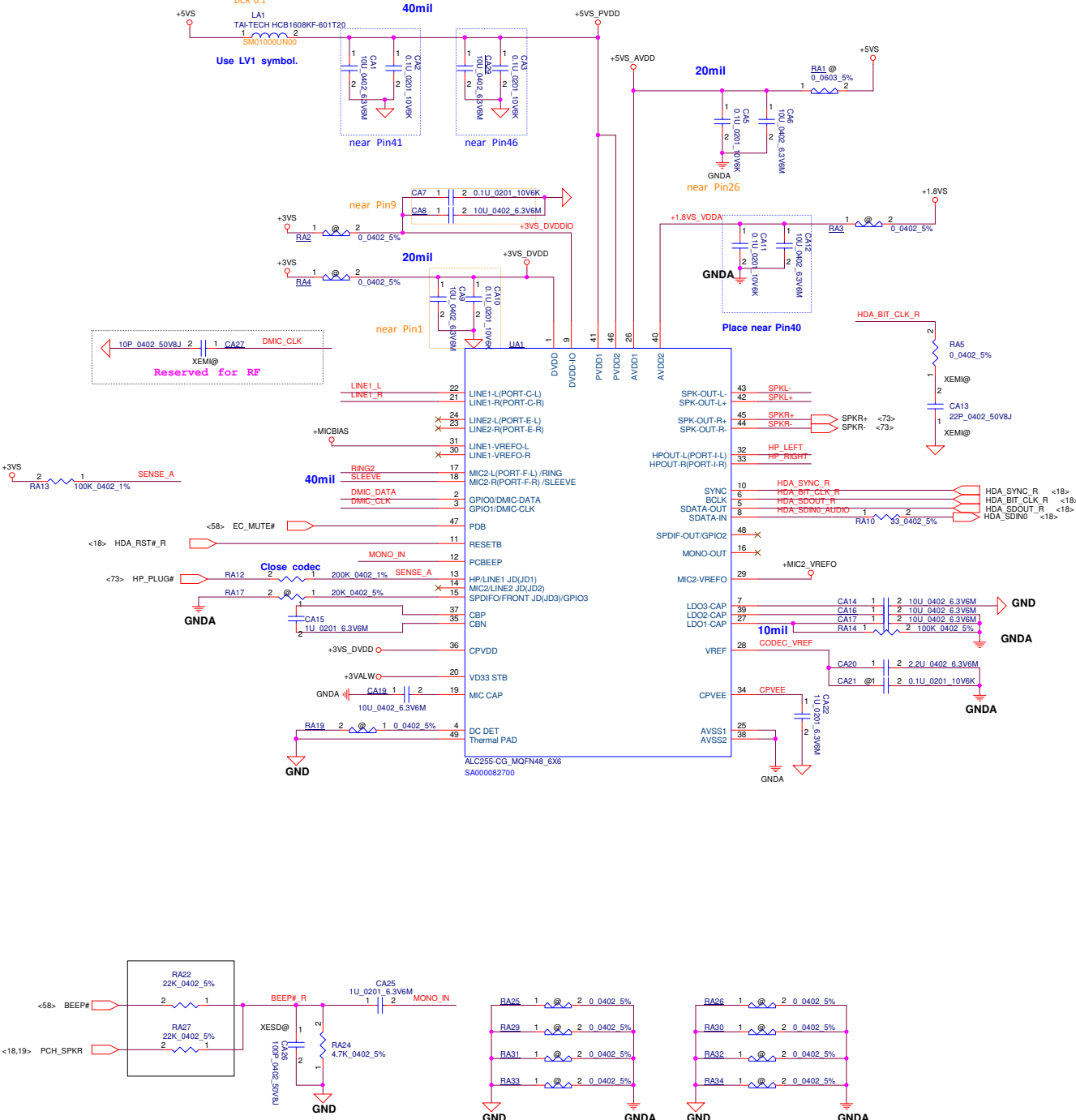
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				Date:	Friday, February 22, 2019
				Sheet	54 of 101
				Rev	1A

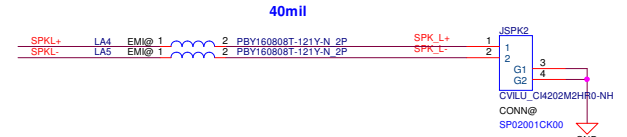
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				EH5VF M/B LA-H501P	
				Date:	Friday, February 22, 2019
				Sheet	55 of 101
				Rev	1A

HD Audio Codec

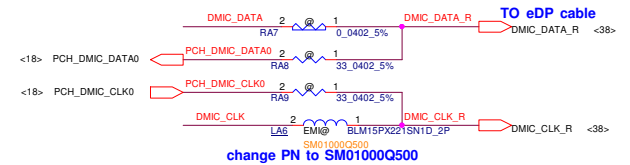


Int. Speaker Conn.

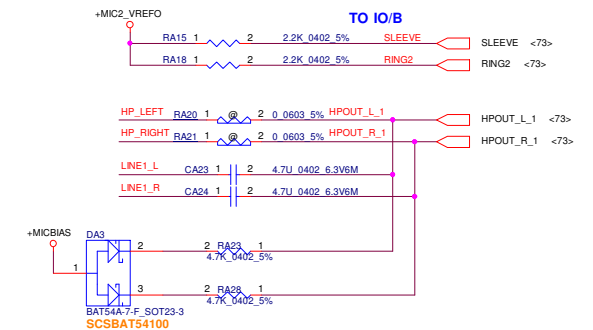


Digital MIC

MIC BOM upload by Audio Team



Headphone Out

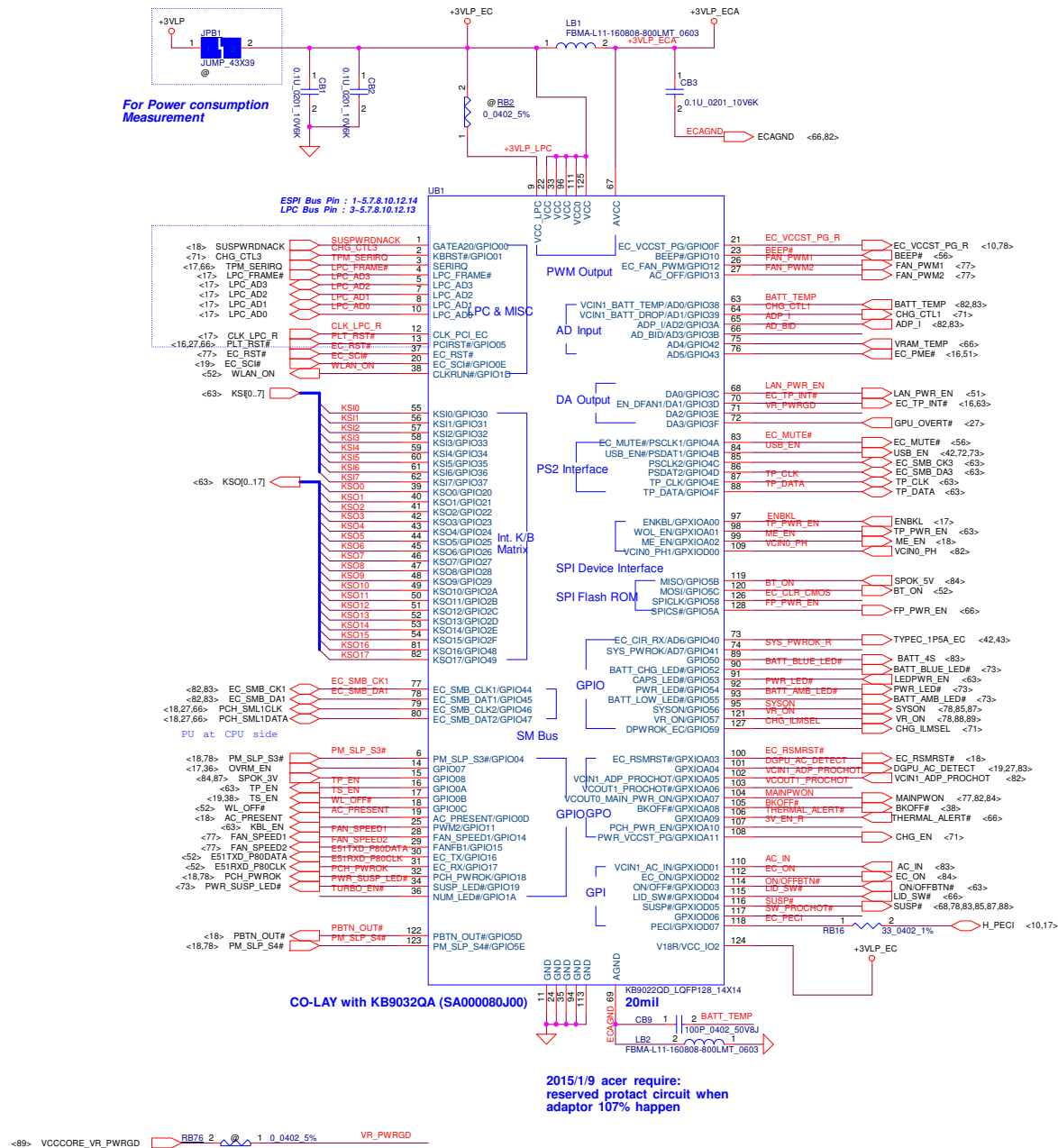
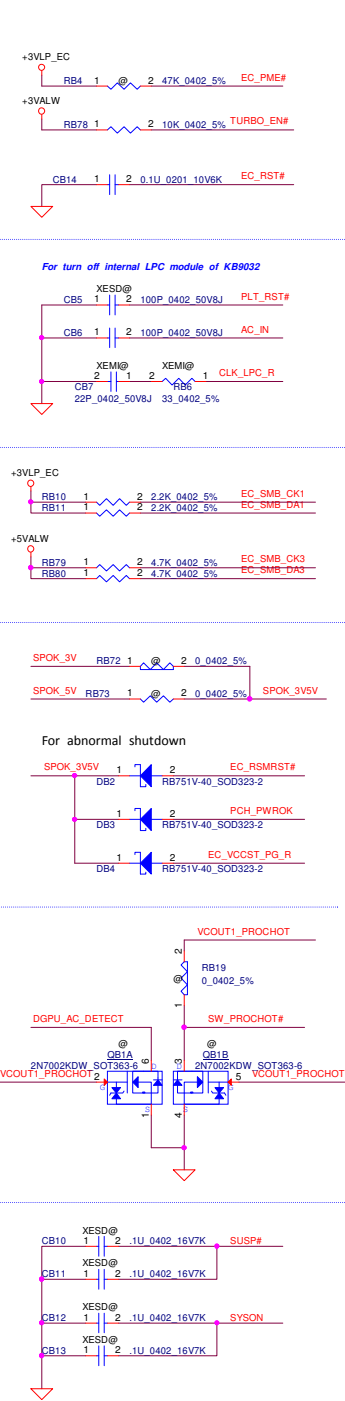


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					Custom	EHSVF M/B LA-H501P		1A	
					Date:	Friday, February 22, 2019	Sheet	56 of 101	

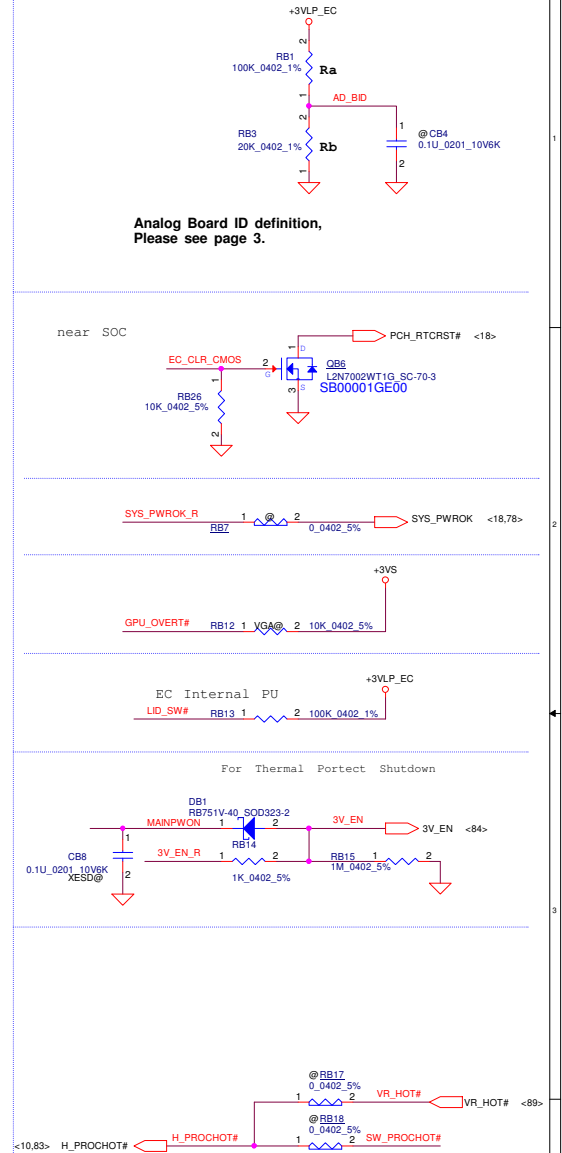
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				EH5VF M/B LA-H501P	
				Date:	Friday, February 22, 2019
				Sheet	57 of 101
				Rev	1A



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Date: Friday, February 22, 2019				Sheet	58 of 101

Reserve Page

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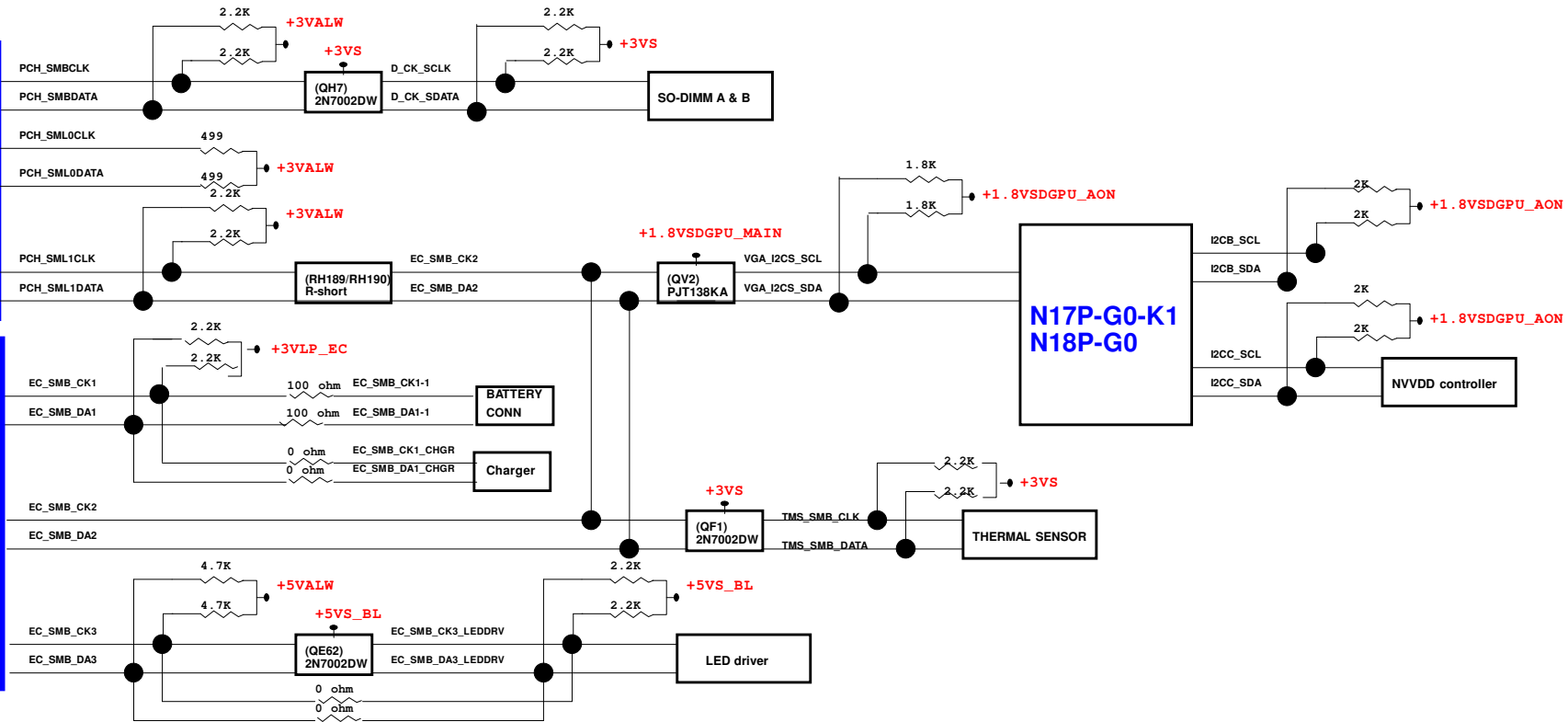
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				EH5VF M/B LA-H501P	
				Date:	Friday, February 22, 2019
				Sheet	59 of 101
				Rev	1A

Reserve Page

Security Classification		Compal Secret Data		Compal Electronics, Inc.	
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				EH5VF M/B LA-H501P	
				Date:	Friday, February 22, 2019
				Sheet	60 of 101
				Rev	1A

Cannonlake
PCH - H

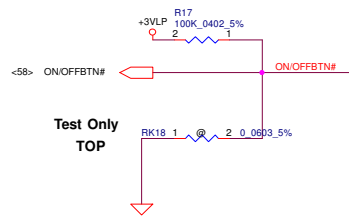
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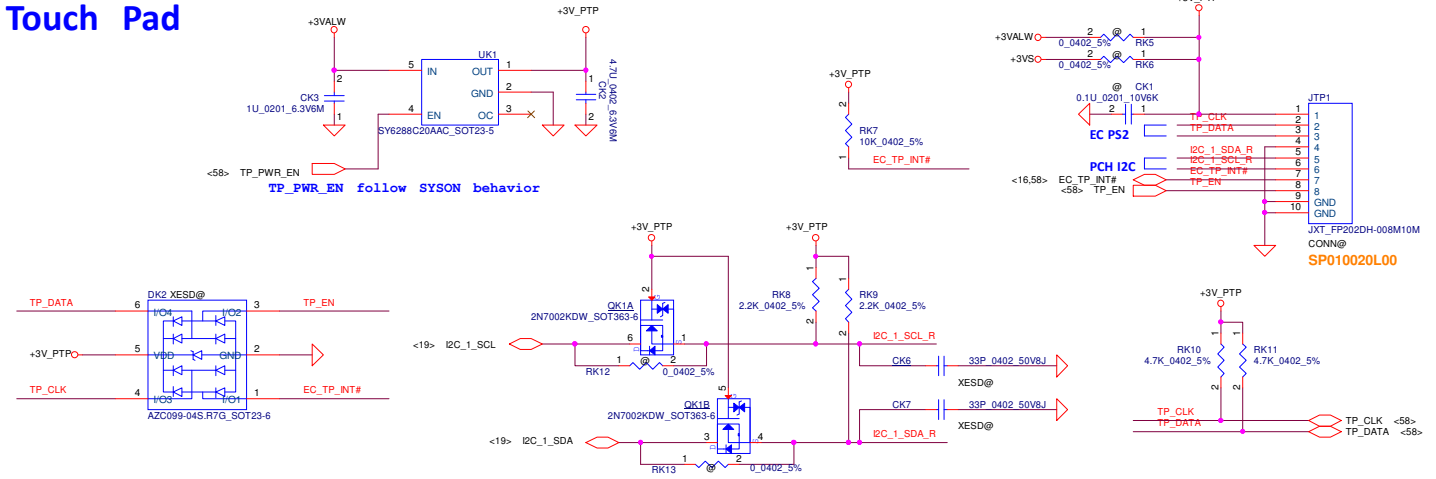
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				EH5VF M/B LA-H501P	
				Date:	Friday, February 22, 2019
				Sheet	62 of 101
				Rev	1A

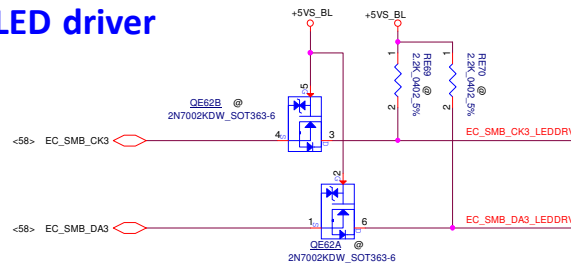
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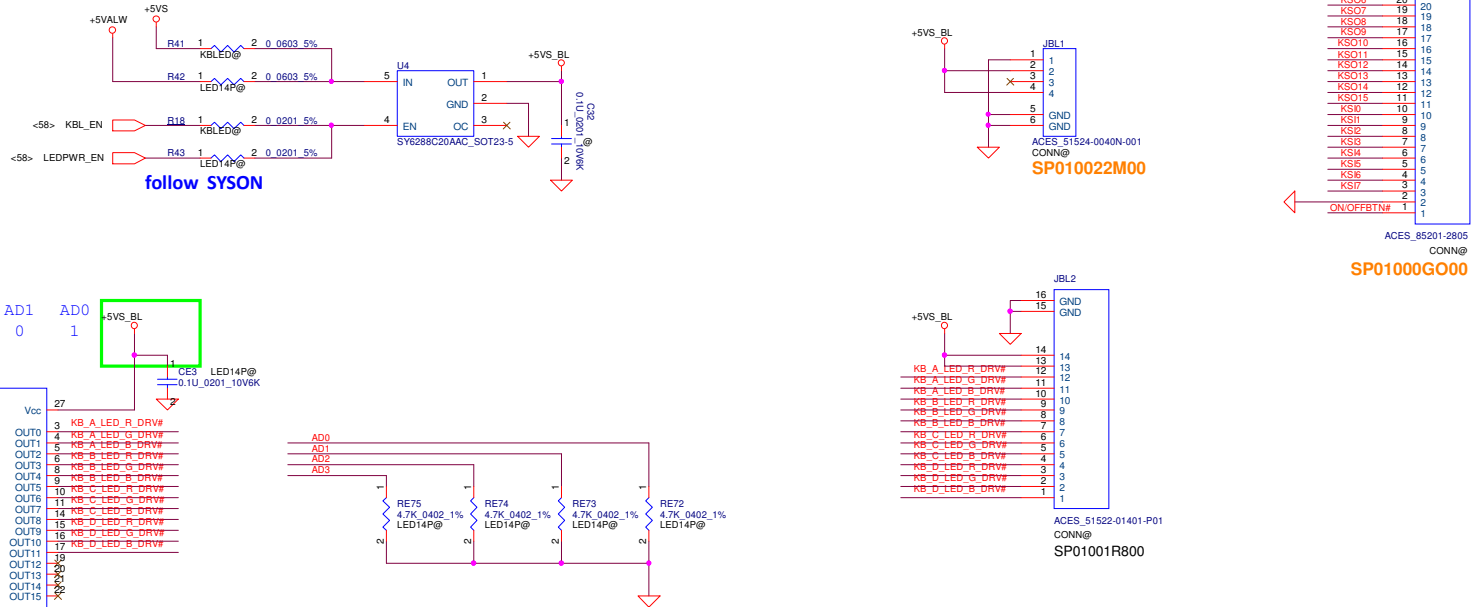
Touch Pad



LED driver



KB Conn. / Backlight



set RE7 to 10k / output = 1.875mA

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				Customer	EH5VF M/B LA-H501P
				Date:	Friday, February 22, 2019
				Sheet	63 of 101
				Rev	1A

Reserve Page

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				EH5VF M/B LA-H501P	
				Date:	Friday, February 22, 2019
				Sheet	64 of 101
				Rev	1A

Reserve Page

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				EH5VF M/B LA-H501P	
				Date:	Friday, February 22, 2019
				Sheet	65 of 101
				Rev	1A

<56> LID_SW#

+3VLP

JHS1

1
2
3
4
5
6
GND
GND

0.1uF
100k

PGESD@

ACES_51524-0040N-001
CONN@

SP010022M00

THERMAL SENSOR

+3VLP_ECA

+3VS

TMS@ CF20 0.1U_0201_10V6K

TMS@ RF24 10K_0402_5%

TMS@ RH250 100K 0402_1%_TSM0B104F4251RZ SL200002H00

TMS@ ECAGND <58,82>

NCT7718W_MSOP8

SMBUS ADDRESS 1001_1000b

TMS_SMB_CLK

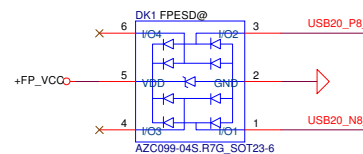
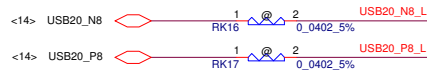
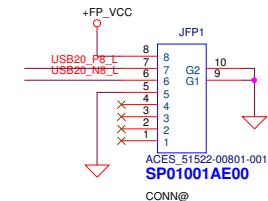
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THERMAL_ALERT# <58>

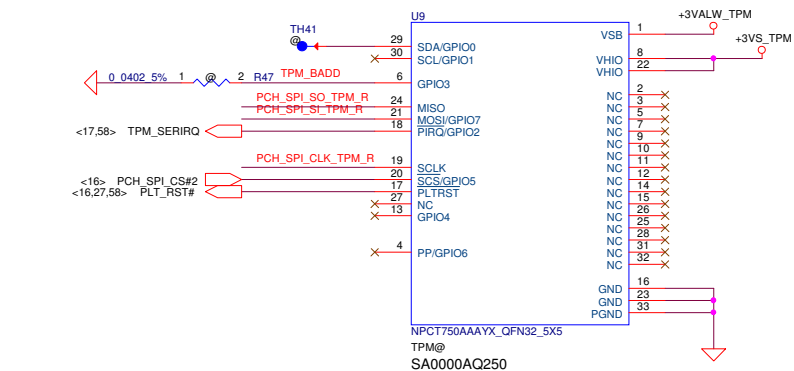
The schematic diagram illustrates the TPM module connections. It shows two TPM modules, TPM0 and TPM1, connected to a +3VALW_TPM supply. TPM0 is connected to PCH_SPI_CS#2 and PCH_SPI_CLK_R. TPM1 is connected to PCH_SPI_SO_TPM_R and PCH_SPI_CLK_TPM_R. The schematic includes various capacitors (C56, C57, C58, C59, C54, C55) and resistors (R45, R46, R48) with their values and tolerances. The TPM modules are labeled 'near pin1' and 'near pin8,22'.

Legend:

- <16> PCH_SPI_SO_R R50 1 TPM@ 2 33 0402 1% PCH_SPI_SO_TPM_R
- <16> PCH_SPI_CLK_R R51 1 TPM@ 2 33 0402 1% PCH_SPI_CLK_TPM_R
- <16> PCH_SPI_CLK_R R52 1 TPM@ 2 33 0402 1% PCH_SPI_CLK_TPM_R



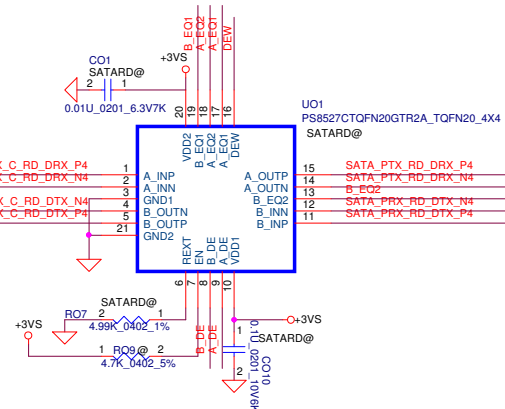
PIN	ETU801	FA577E-1200
1	+FP_VCC (5V)	+FP_VCC (3V)
2	USBP	D+
3	USBN	D-
4	GND	GND
5	NC	NC
6	NC	NC
7		NC
8		NC



SA0000AQ250, S IC NPCT750AABYX QFN 32P TPM

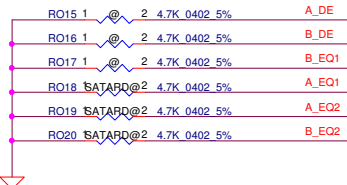
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				Size	Document Number	Rev
				Date: Friday, February 22, 2019 Sheet 66 of 101		

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Chip Enable, Internally pulled up at ~150KΩ

EN	Status
L	Chip disabled
H	Chip enabled(default)



Programmable output de-emphasis level setting for channel B.
(Internally tied to VDD/2(M status))

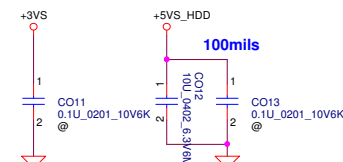
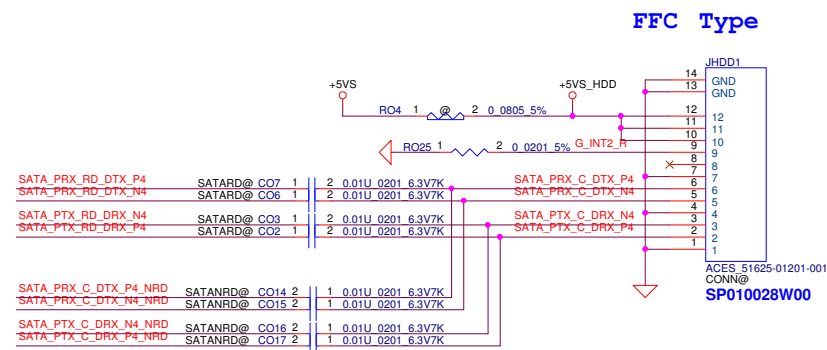
A_DE	De_Emphasis
M	-3.5dB(Default)
L	0dB
H	-6dB

B_DE	De_Emphasis
M	-3.5dB(Default)
L	0dB
H	-6dB

Equalizer control and program for channel B.
Internally tied to VDD/2(M status)

A_EQ2	A_EQ1	EQ for channel loss
L	M	2.4dB
L	L	7.4dB
L	H	14.4dB
M	M	12.2dB(default)
M	L	9.4dB
M	H	13.3dB
H	M	6.2dB
H	L	11.2dB
H	H	5dB

B_EQ02	B_EQ01	EQ for channel loss
L	M	2.4dB
L	L	7.4dB
L	H	14.4dB
M	M	12.2dB (default)
M	L	9.4dB
M	H	13.3dB
H	M	6.2dB
H	L	11.2dB
H	H	5dB



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					Size	Document Number	Rev
					Custom	EH5VF M/B LA-H501P	1A
Date:					Friday, February 22, 2019	Sheet	67 of 101

Reserve Page

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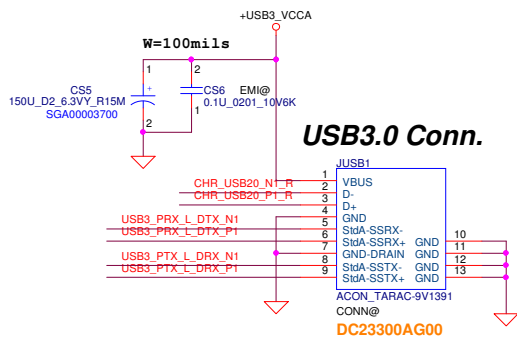
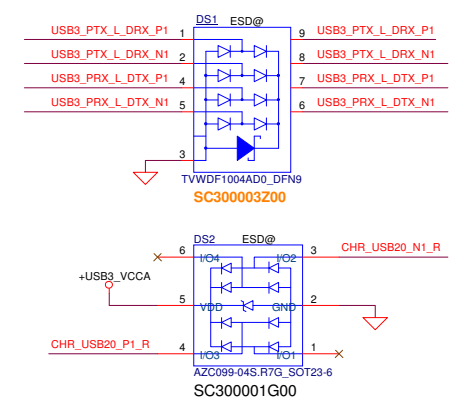
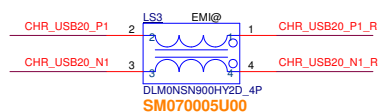
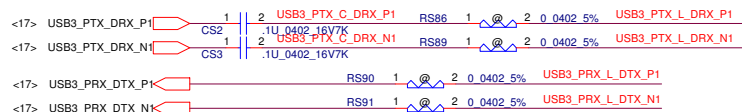
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				EH5VF M/B LA-H501P	
				Date:	Friday, February 22, 2019
				Sheet	69 of 101
				Rev	1A

Reserve Page

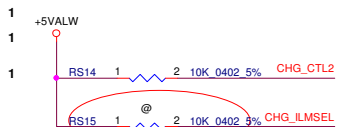
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				EH5VF M/B LA-H501P	
				Date:	Friday, February 22, 2019
				Sheet	70 of 101
				Rev	1A

USB3.0



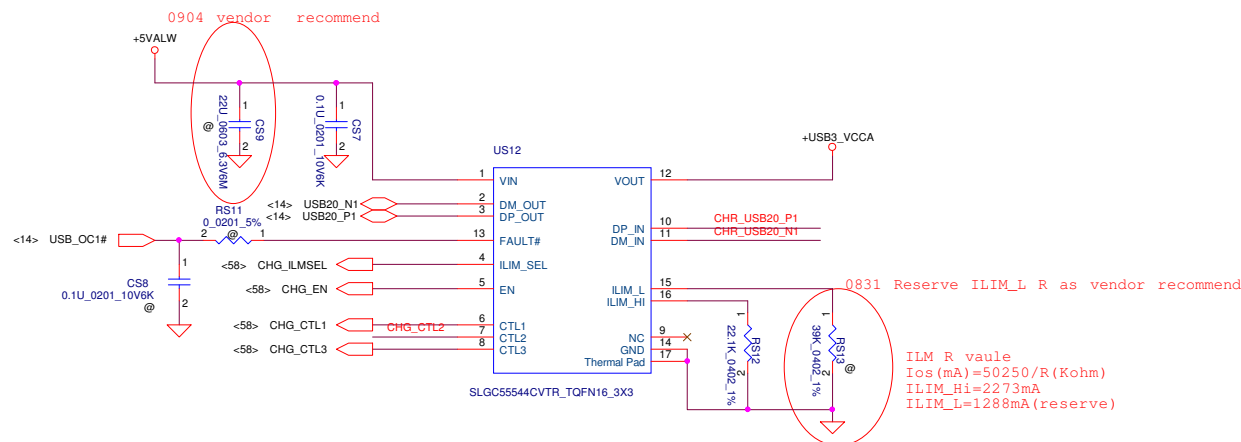
USB Host Charger



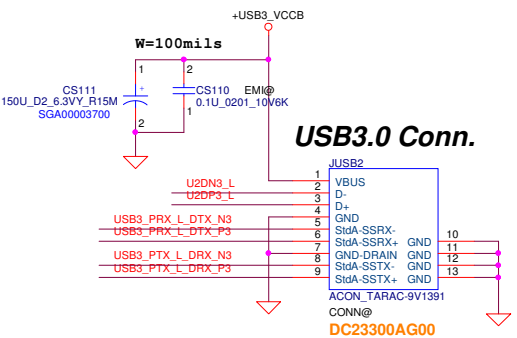
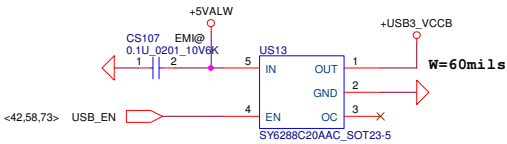
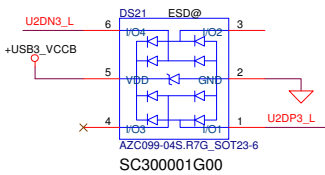
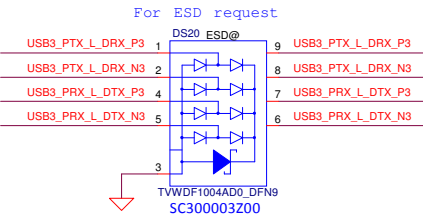
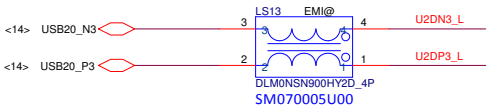
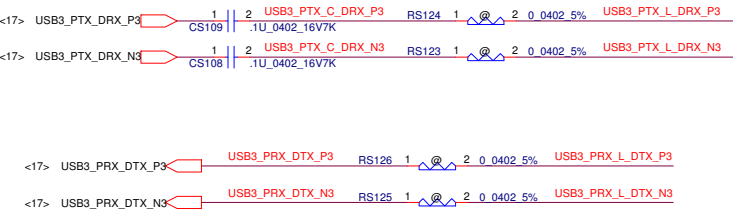
0911 Reserve PU, vendor suggest to EC control if future need support SDP2

USB Host Charger Truth Table

CHG_EN	CTL1	CTL2	CTL3	ILIM_SEL	MODE	Current Setting	Limit	Note
0	1	0	1		SDP1-OFF	ILIM_H		Port power off
0	1	0	1		SDP1	ILIM_H		Data Lines Connected
0	1	1	1		DCP Auto	ILIM_H		Data Lines Disconnected
1	1	1	1		CDP	ILIM_H		Data Lines Connected

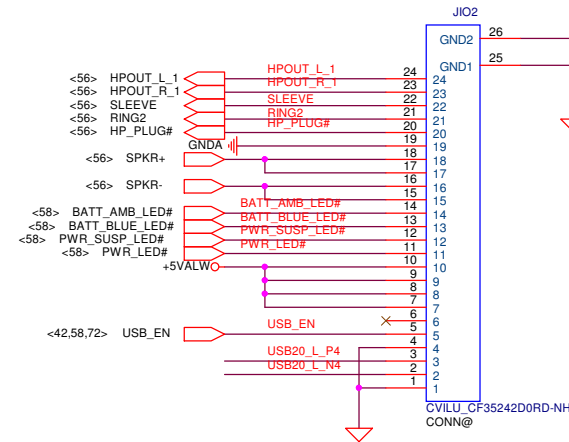
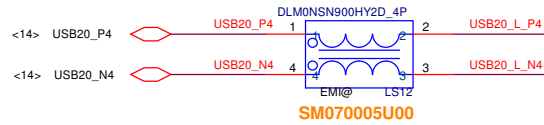


USB3.0



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				Date	Friday, February 22, 2019
				Sheet	72 of 101
				Rev	1A

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				Date: Friday, February 22, 2019	Sheet 73 of 101
				EH5VF M/B LA-H501P	
				Rev 1A	

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				Date:	Friday, February 22, 2019
				Sheet	74 of 101
				Rev	1A

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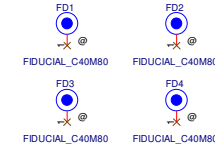
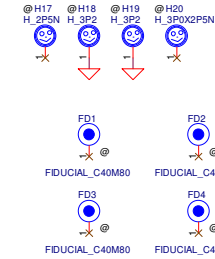
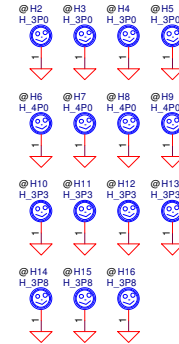
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				EH5VF M/B LA-H501P	
				Date:	Friday, February 22, 2019
				Sheet	75 of 101
				Rev	1A

Reserve Page

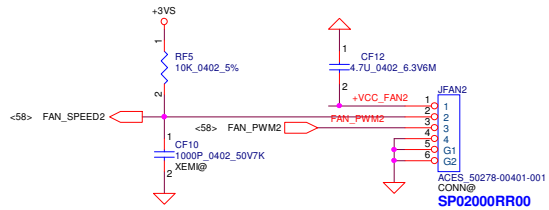
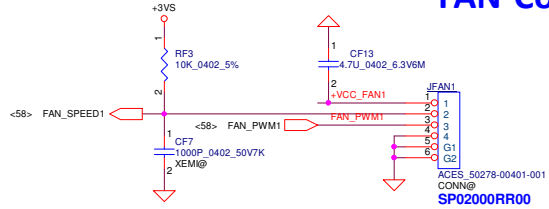
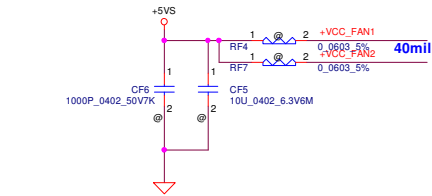
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				EH5VF M/B LA-H501P	
				Date:	Friday, February 22, 2019
				Sheet	76 of 101
				Rev	1A

Screw Hole

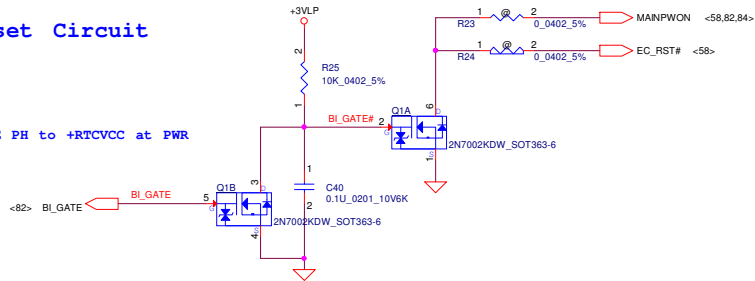


FAN Conn

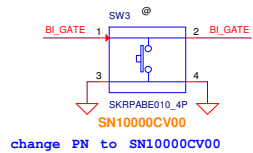


Reset Circuit

BI_GATE PH to +RTCVCC at PWR side

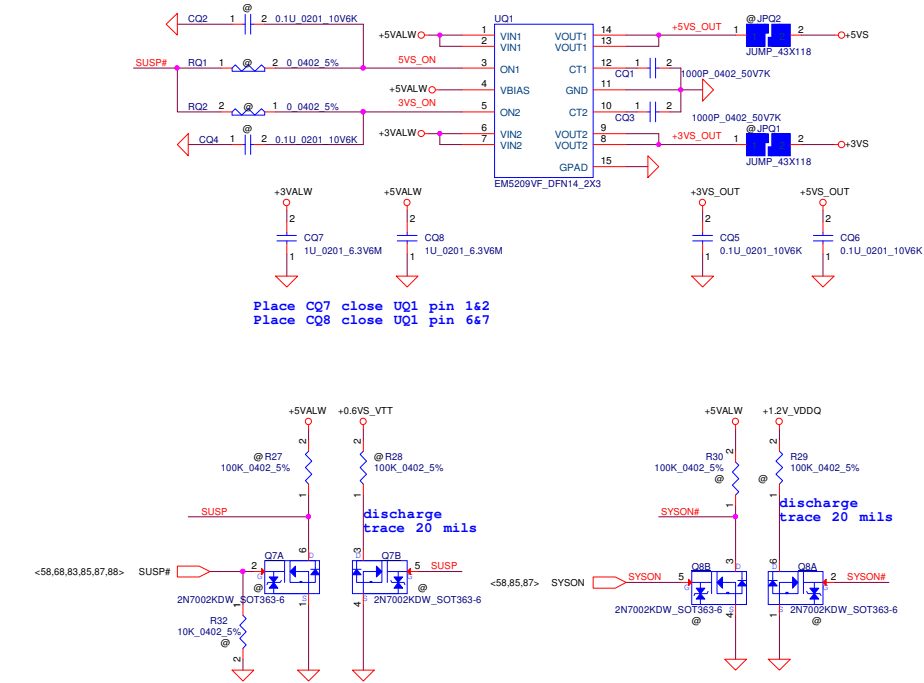


Reset Button

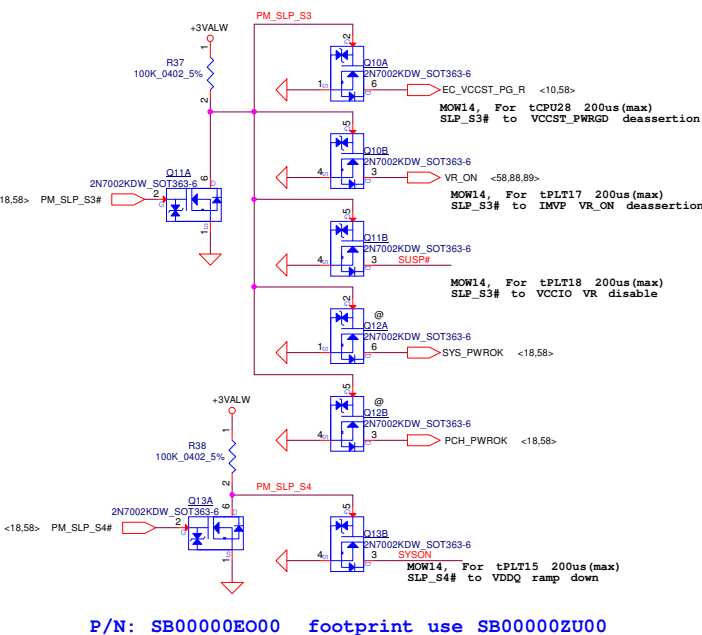


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				Custom	EH5VF M/B LA-H501P
				Date:	Friday, February 22, 2019
				Sheet	77 of 101
				Rev	1A

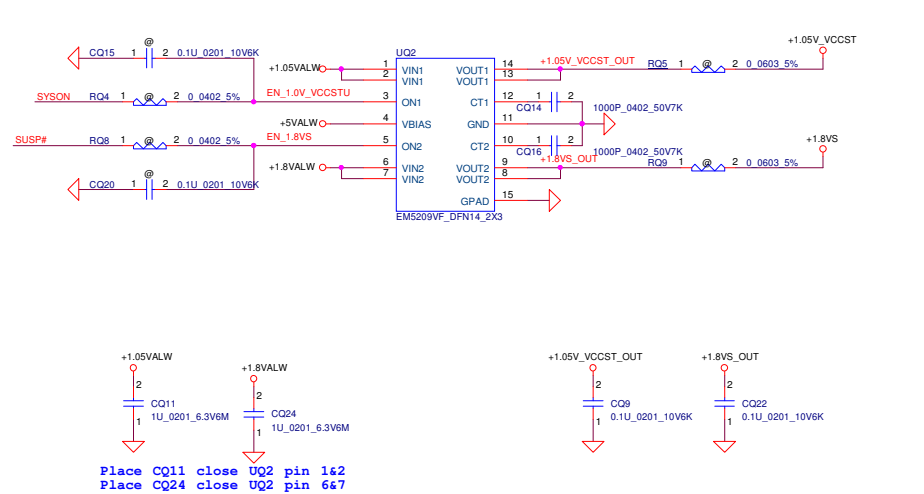
System DC interface



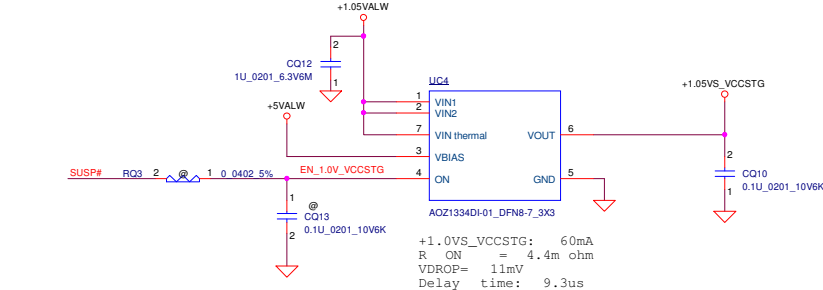
For Power ON/Off Sequence



+1.05VALW TO +1.05V_VCCST /+1.8VALW TO +1.8VS



+1.05VALW TO +1.05VS_VCCSTG

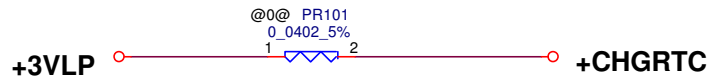
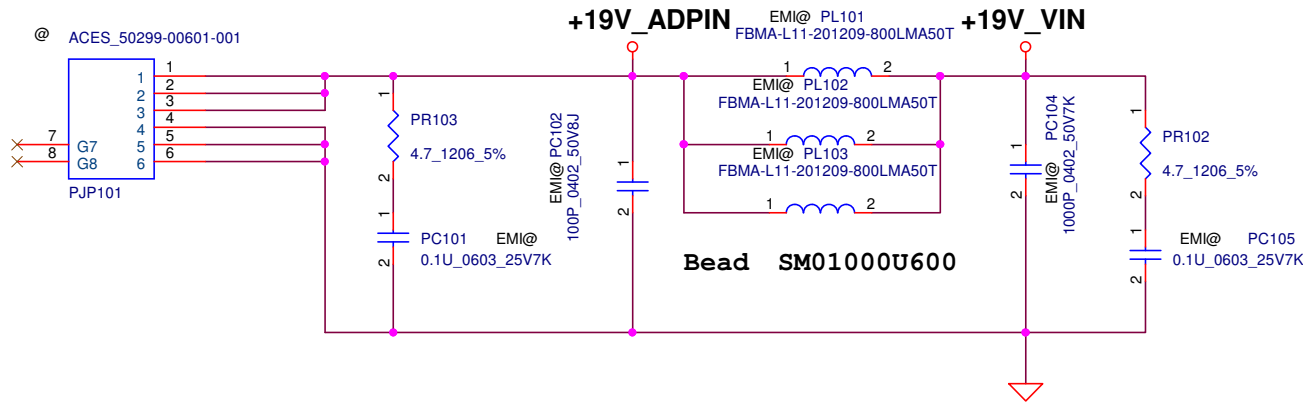


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				Rev	
				1A	
Date:		Friday, February 22, 2019		Sheet	79 of 101

Reserve Page

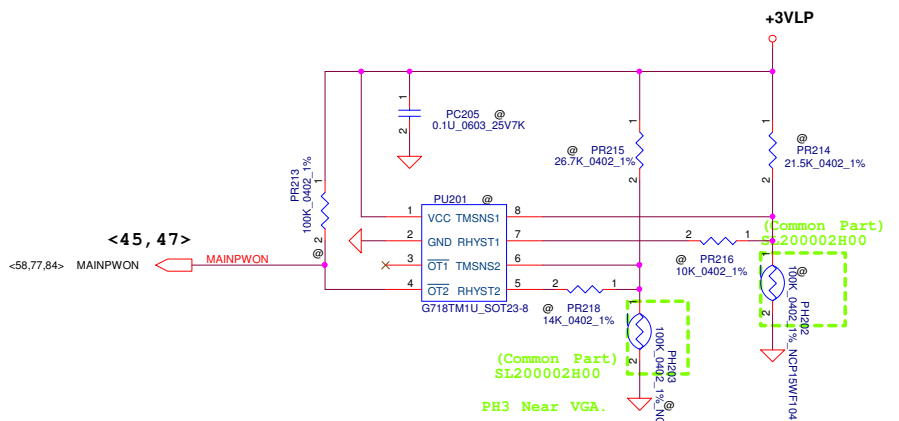
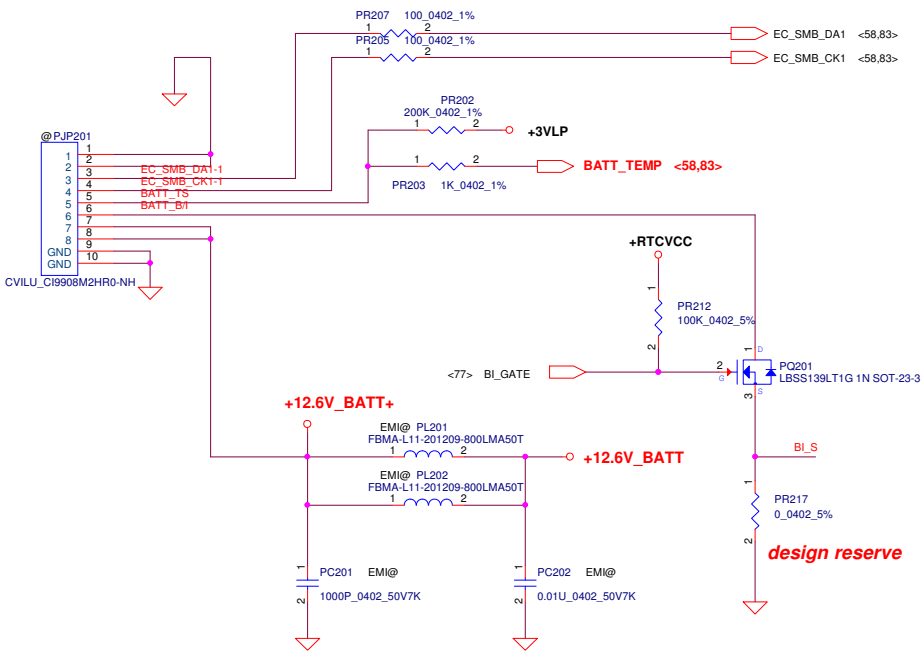
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				EH5VF M/B LA-H501P	
				Date:	Friday, February 22, 2019
				Sheet	80 of 101
				Rev	1A



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				Date:	Friday, February 22, 2019
				Sheet	81 of 100

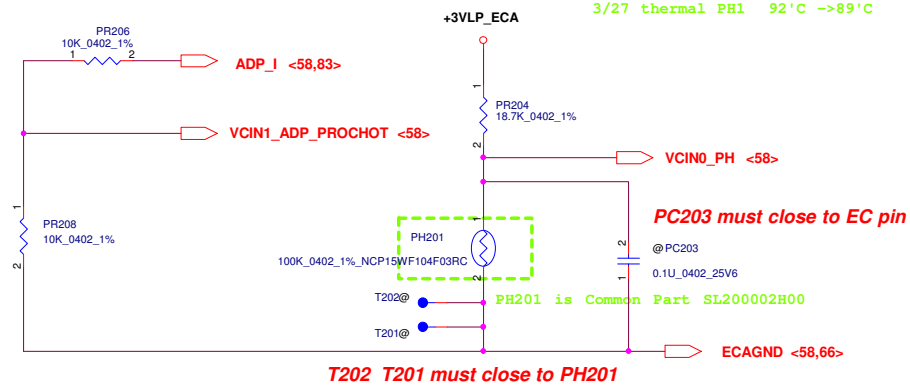
Battery Bot Side

PIN1 GND
PIN2 GND
PIN3 SMD
PIN4 SMC
PIN5 TEMP
PIN6 BI
PIN7 Batt+
PIN8 Batt+



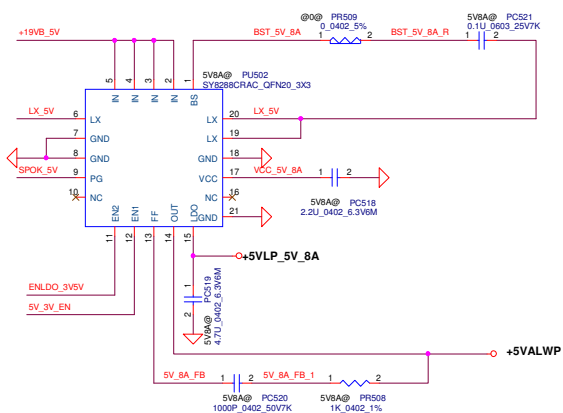
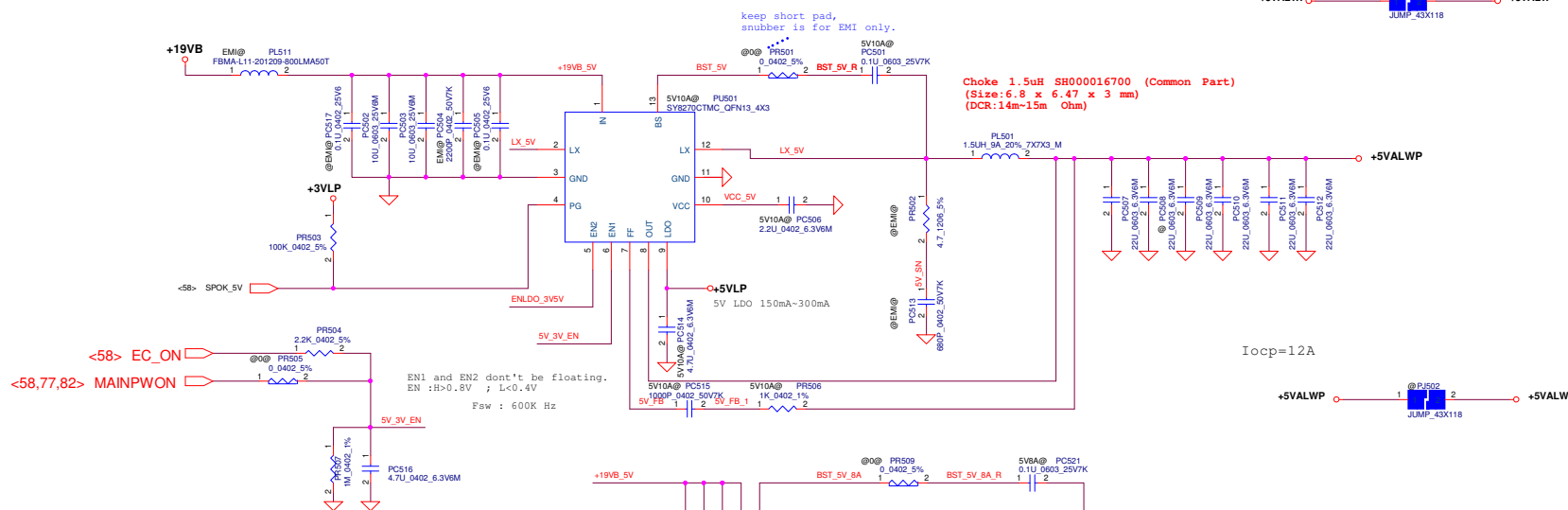
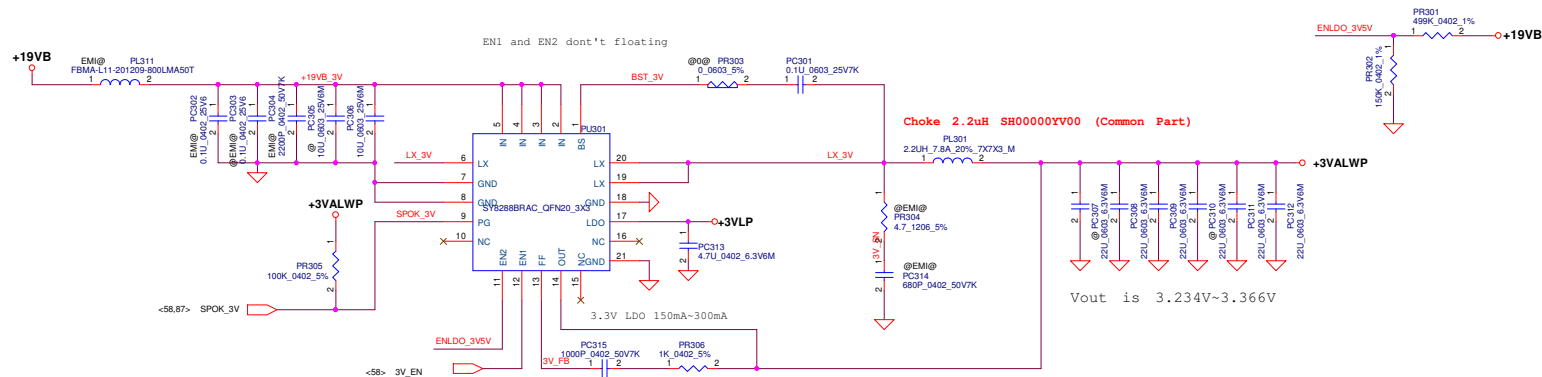
When PR204=18.7K

For KB9022 OTP	Active	Recovery
VCIN0_PH(V)	89'C, 1V	56'C, 2V
PH202 (ohm)	8.0524K	26.11K



$$ADP_I = 20 * I(\text{adapter}) * 0.01$$
$$I(\text{adapter}) = \text{adapter (W)} * 130\% / 19$$

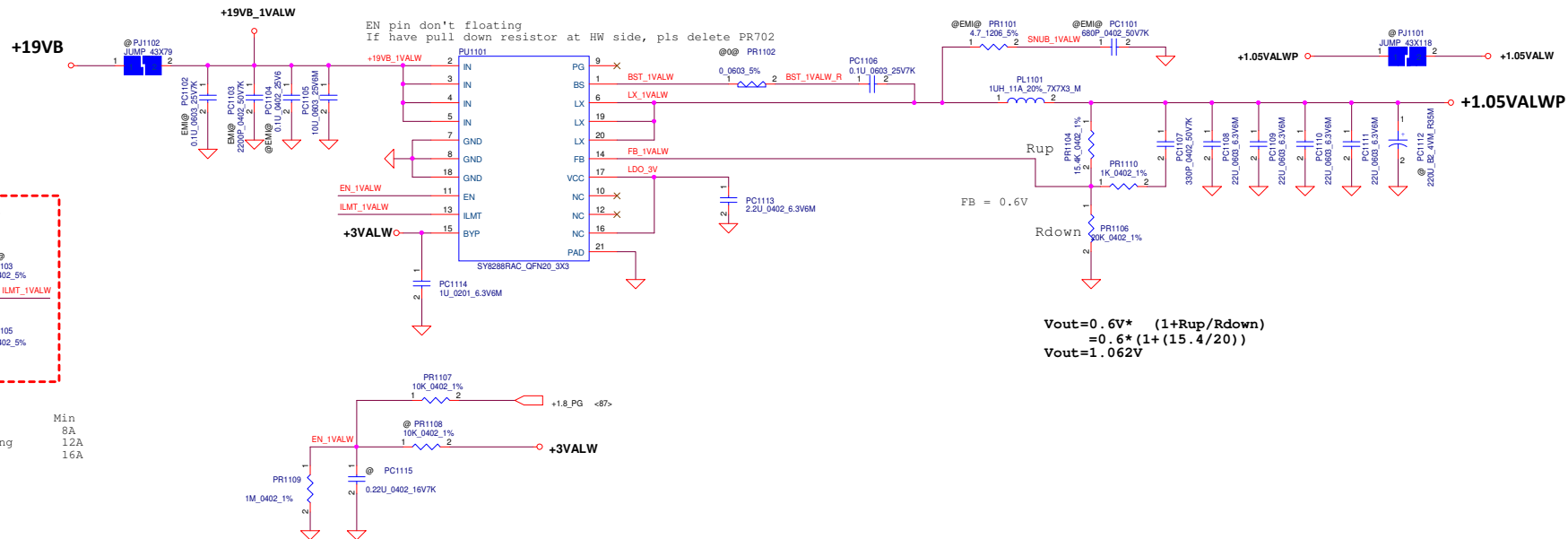
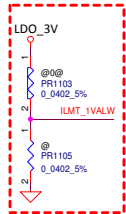




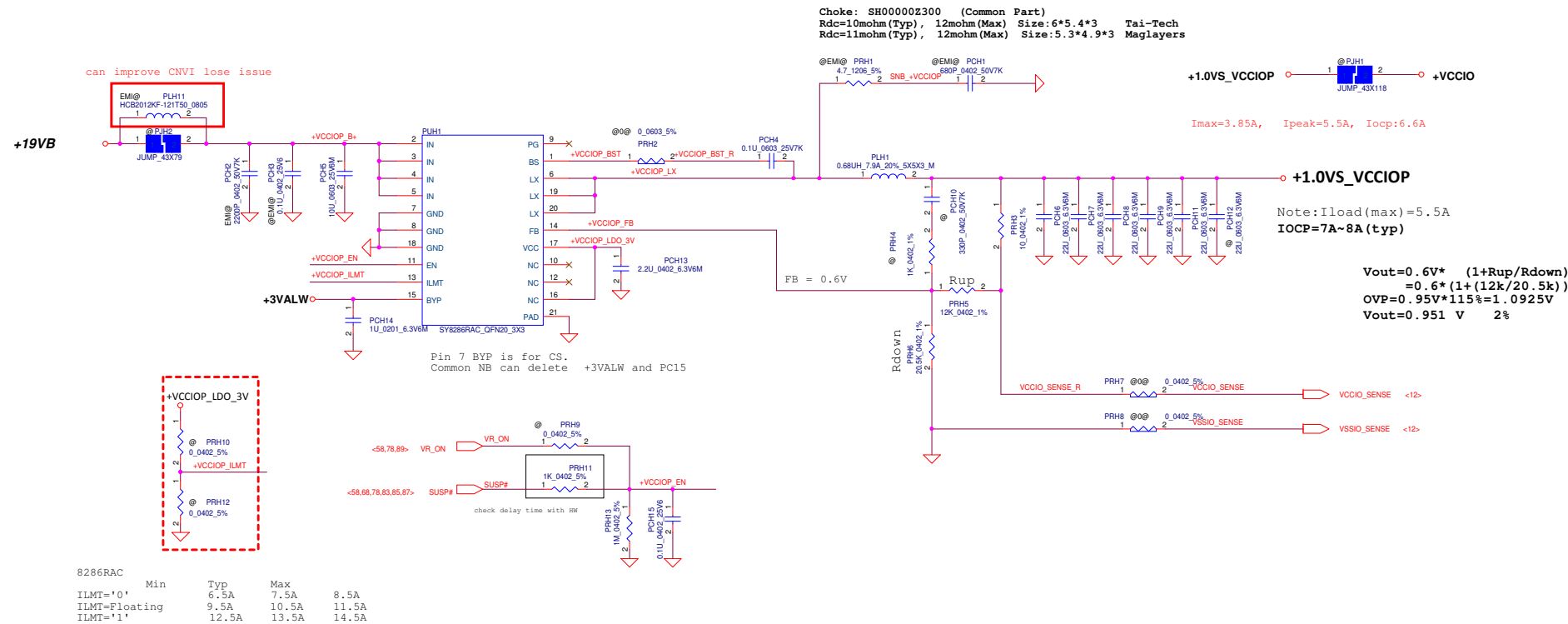
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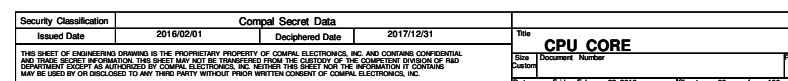
8288RAC
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Min
8A
12A
16A

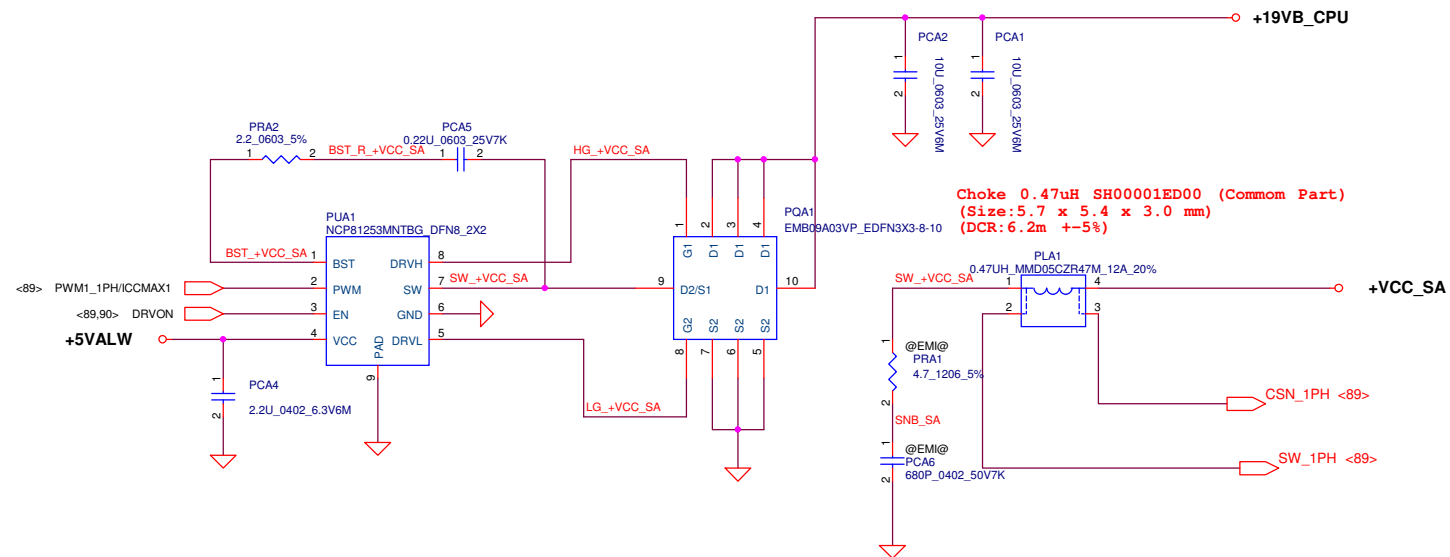
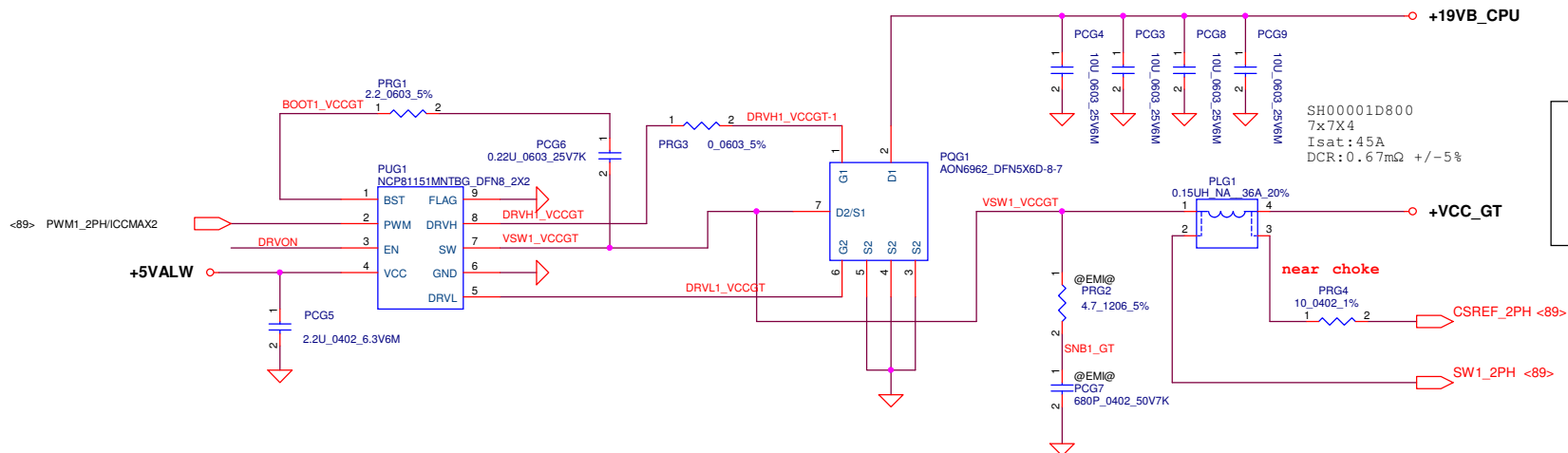


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				Date:	Friday, February 22, 2019
				Sheet	86 of 100
				Rev	1A





Main Func = VCCGT/+VCCSA

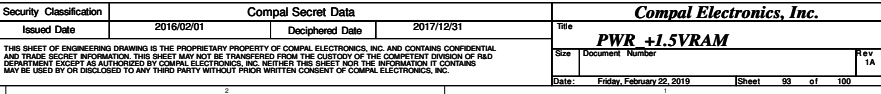


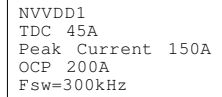
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Size	Document	Number	CIPRG LA-E051P		Rev 1A
Date:	Friday, February 22, 2019	Sheet	91	of	100


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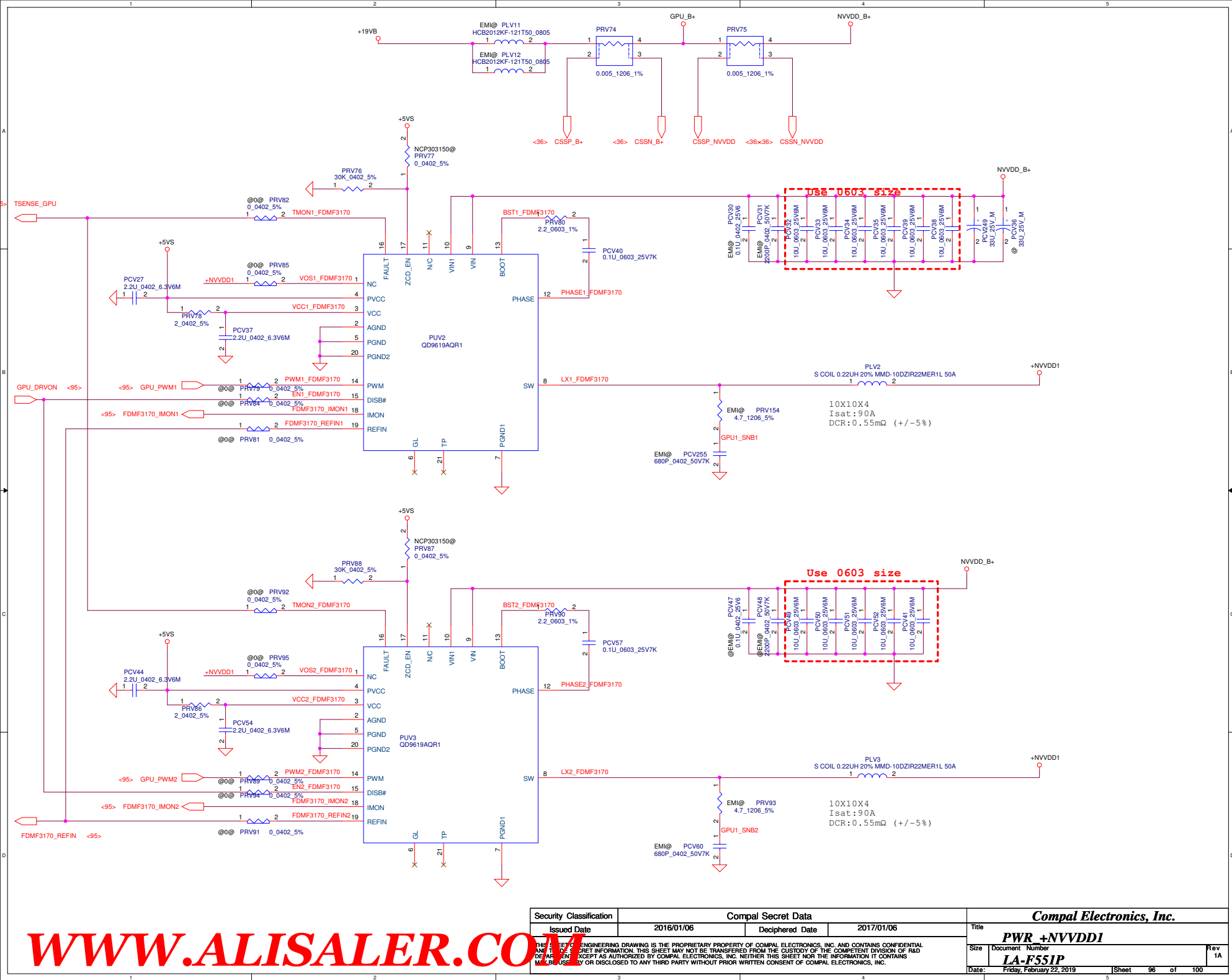
Micron & Hynix VRAM
When, VRAM_VDD_CTL=High
Vboot=2*30.9K/(10K+30.9K+80)
=1.51V
When, VRAM_VDD_CTL=Low
Vboot=2*(30.9K//68.1K)/(10K+(30.9K//68.1K)+80)
=1.36V

```





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				Size	Document Number
				LA-F551P	
Date:				Friday, February 22, 2019	Sheet 95 of 100

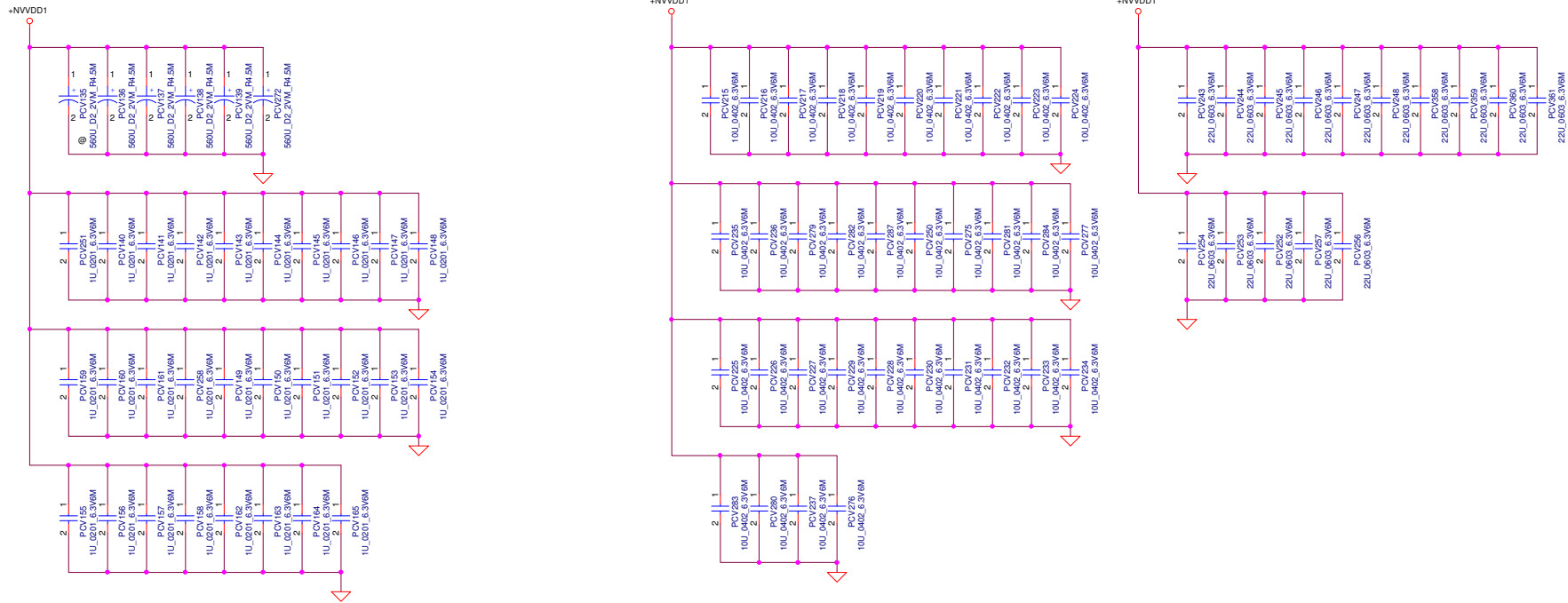


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				1A	LA-F551P
				Date	Friday, February 22, 2019
				Sheet	96 of 100

N18P-G0
+NVVDD
560uF X 6
22uF_0603 X 15
10uF_0402X 34
1uF_0201 X 28

Rail (GPU Ball) Name	Balls	Voltage	Filtering under GPU	Filtering Near GPU
GB4B-256 Package				
NVVDD		Varies	185 X 0.47uF (0201W X65)	2 X 470uF (Pocap)
			23 X 10uF (0603 X65)	
			4 X 22uF (0805 X65)	
			3 X 47uF (0805 X65)	
FBVDDQ (GPU side) ¹		1.25V	48 X 0.47uF (0201 X65)	7 X 10uF (0603 X65)
		1.35V	5 X 10uF (0603 X65)	9 X 22uF (0603 X65)
		1.5V		
		1.55V		



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				Date:	Friday, February 22, 2019
				Sheet	97 of 100

Reserve Page

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				Date:	Friday, February 22, 2019
				Sheet	98 of 100
				Rev	1A

Reserve Page

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				EH5VF M/B LA-H501P	
				Date:	Friday, February 22, 2019
				Sheet	99 of 100
				Rev	1A

Item	Fixed Issue	Reason for change	PG#	Modify List	Date	Phase
01	Design Update	For EA Turning and HW sequence	93, 94 95, 97 89, 92	change PR1009 from 100K_0402_5% (SD028100380) to 10K_0402_5% (SD028100280) change PG pull high from +3VS to +3VALW change PRW1 from 20K_0402_1% (SD034200280) to 1K_0402_1% (SD034100180) Change the PCW27 from pop to un-pop, and . PCW27.2 net name change from +1.35VSDGPU to Vsense_+1.35VS_VGAP. unpop PCV135 Change the PUV8, PCV9 from pop to un-pop. Add location PRV51 0_0402_5% (SD028000080), and pop. Change the PCW21, PCW22 From 4700P_0402_50V (SE074472K80) to 2200P_0402_50V(SE074222K80). Delete PL1111 (HCB2012KF-121T50_0805)	11/14	A
02	Design Update	solution change	83, 85 90, 91	Change the PQB2,PQM2 from AON7506 (SB000010A00) to EMB12N03V (SB00001HV00) update location PR65 PRA3 to PUG1 PUA1 PLZ1,PLG1,PLZ2,PLZ3,PLZ4 change to common part P/N (SH00001EE00) pop PQZ2, PQZ4 unpop PQZ1, PQZ3	11/16	A
03	Design Update	0 ohm to R-short	83, 85 90, 91	Change PRM10, PRM8, PRV82, PRV85, PRV92, PRV95, PRV79, PRV81, PRV84, PRV89, PRV91, PRV94, PRV54, PRV56, PRV70, PRV145, PRV146, PRZ72, PRZ73, PRZ25, PRZ30, PRZ32, PRZ18, PRZ9, PRZ11, PRZ24, PRZ27,PRV20, PRV34	11/16	A
04	Design Update	For CPU transient	89, 92	change PRZ12 from 1.78K_0402_1%(SD00000WY80) to 1.62K_0402_1%(SD000003380) change PRZ14 from 31.6K_0402_1%(SD034316280) to 28K_0402_1%(SD034280280) change PCZ24 from 470P_0402_50V8J(SE071471J80) to 220P_0402_50V8J(SE082221J80) change PRZ51 from 84.5K_0603_1%(SD014845280) to 100K_0603_1%(SD014100380) PRZ61=110k ohm @H82, PRZ61=102k ohm @H62 PRZ35=25.5k ohm @H82, PRZ35=28k ohm @H62 unpop PCZ101, PCZ103, PCG102 pop PCZ176 un pop PCZ120, PCZ104, PCZ105, PCZ118, PCZ111, PCZ108, PCZ126, PCZ124 for H82 un pop PCZ120, PCZ104, CZ105, PCZ118, PCZ111, PCZ108, PCZ126, PCZ124, PCZ123, PCZ127, PCZ107, PCZ113, PCZ116, PCZ114 for H62	11/19	A
05	Design Update	solution change	84	Change the PL501 1.5uH to common part Change the PCZ47, PCZ48, PCZ65, PCV36, PCV249 from 33U_25V_NC_6.3X4.5 (SF000007200) to 33U_25V_M (SF000007700) Chnage the PRZ43 from 12.1K_0402_1% (SD034121280) to 12K_0402_1% (SD034120280)	12/3	A
06	Design Update	solution change	87	unpop PC1811 0.47U_0402_6.3V6K (SE124474K80)	12/12	B
07	Design Update	solution change	83, 97	pop PCV149~PCV158, PCV162~PCV165, PCV258 (1U_0201_6.3V6M) reserve PDB2 for dead battery	12/18	B
08	Design Update	solution change	87, 93, 94	Change PR1010, PRW9, PR1801, PR2501 from 0ohm to r-short	12/18	B

Item	Page	Title	Date	Issue Description	Solution Description	Phase	Rev.
1	6	Chipset	11/14	Update CPU,PCH,GPU PN.		DVT	0.2
2	43,68, 71,72	Source	11/14	Change material source.	1.Change CS95,CM3,CM20,CS5,CS111 to SGA00003700.	DVT	0.2
3	58	EC	11/14	Design change.	1.Add CB14 on EC_RST#.	DVT	0.2
4	27,37	GPU	11/14	Design change and fine tune sequence.	1.Remove RV397, pop RV335. 2.Reserve CV400, change RV106 to 100kohm. 3.Change RV105 to 10kohm, CV197 to 0.22uF, depop DV4. 4.Change RV22 to 200kohm. 5.Change UV45,UV48 to SA000070V00.	DVT	0.2
5	66	Sensor	11/15	Design change.	1.Remove R39,R40,C41,U6.	DVT	0.2
6	58	EC	11/16	Board ID.	1.Change RB3 to 12kohm.	DVT	0.2
7	43,56	Source	11/16	Change material source.	1.Change CS13 to SE00000X200,0603 size. 2.Change DS19 to SCA00004500. 3.Change LA4,LA5 to SM01000BW00. 4.Change UF2 to SA000067P00. 5.Change QV3,QV4 to SB00001GC00. 6.Change UH3 to SA000000H00. 7.Change UC3 to SA00007WE00.	DVT	0.2
8	32	VRAM	11/19	For N17P-G0-K1 SKU.	1.Change UV4 related component BOM structure to VRAM4G@.	DVT	0.2
9			11/20	Design change.	1.Change RV338,RH94,RH96,RH99,RH101,RH102,RH103,RH105,RX8,RX9 to R-short.	DVT	0.2
10	67	HDD	11/20	Follow DVR1012,HDD CONN P11 pull-down.	1.Add RO25, remove T211.	DVT	0.2
11	10	ESD	11/21	For ESD request.	1.Add CC101,CC102,CC103, change CD10 to 33pF and pop.	DVT	0.2
12	27,51	Crystal	11/21	By Crystal EA result.	1.Add RL14, change CL21,CL22 to 18pF. 2.Change RV80 to 470ohm, CV1,CV2 to 18pF.	DVT	0.2
13	43	TYPEC	11/23	Update CONN symbol.	1.Change JTYPEC1 to DC23300RC00.	DVT	0.2
14	42,43 ,58	TYPEC	12/18	Follow 2018 Type-C spec.	1.Remove RS127, add US14. 2.Remove TYPEC_1P5A net from PCH. 3.Add TYPEC_1P5A_EC net from EC. 4.Add RS137.	DVT	0.3
15	36	GPU	12/18	OVRM issue.	1.Change RV399 power source to +3VLP. 2.Change RV345~RV348,RV370,RV371,RV372,RV374 power rail to +3V_OVRM. 3.Add QV16,RV400,OVRM_EN net to EC/PCH, reserve RH261.	DVT	0.3
16	58	EC	12/18	Update board ID.	1.Change RB3 to 15k.	DVT	0.3
17			12/27	Design change.	1.Change RA7,RQ1,RQ2,RQ3,RQ4,RQ8,RV352,RV353,RV356,RV358,RV362,RV364,RV365,RV382,RM53 to R-short.	PVT	1.0
18	63,77	ESD/EMI	01/03	For ESD/EMI request.	1.Reserve DK2,CK6,CK7 for ESD. 2.Add SPRING1~3 for EMI.	PVT	1.0
19	58	EC	01/03	Update board ID.	1.Change RB3 to 20k.	PVT	1.0
20	66	ESD	01/31	For ESD request.	1.Add C60.	PVT	1A

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